# Comparison of FIR Filter Lengths and Adaptation Methods in Digital Active EMI Filters based on Delay-Compensated Digital Gate Control Signals

Maximilian Lemke, Tobias Dörlemann, Robert Nowak, Jens Aigner, Stephan Frei

On-board Systems Lab, TU Dortmund University, Germany

maximilian.lemke@tu-dortmund.de

***Abstract* — Modern motor inverters use steep switching waveforms to reduce losses and high switching frequencies for a high power density. This makes inverters potential sources of electromagnetic interference (EMI), which is usually reduced by large and heavy passive EMI filters. The idea of Active EMI Filters (AEF) is to reduce size and weight of the passive filter circuit. Digital Active EMI Filters (DAEF) based on FIR (finite impulse response) filter structures can achieve very high performance when used in feed-forward mode with an estimated, predicted anti-noise signal. Hereby, the anti-noise signal is calculated by a FIR filter, whose input signal is the superposition of the digital gate control signals. The time required to calculate and inject the anti-noise signal is compensated by adding a short delay to the digital gate control signals before arriving at the gate driver. In this work, a comparison of different FIR filter lengths and adaptation methods for Common Mode (CM) EMI reduction in a motor drive system is presented. A further development of the delayed digital control (DDC)-DAEF implementation is introduced, in which the filter weights are calculated iteratively using the Wiener-Hopf-equation. Results are presented and discussed for a freewheeling and a mechanically loaded inverter-motor system.**

***Keywords* —Active EMI filter, Digital Active EMI filter, Adaptive Filter Theory, FIR filter, DC-AC power converters, inverters, EMC, power electronics, motor drives.**

## I. Introduction and Motivation

Modern electric powertrain systems make use of steep switching waveforms to reduce losses and high switching frequencies to increase power density. This combination leads to a broadband EMI spectrum with high noise levels. Usually, passive EMI filters are used to reduce EMI, but their size lowers the power density and increases weight. Therefore, **A**ctive **EMI** **F**ilters (AEFs) were introduced to reduce the size and weight of the overall filter circuit [1].

Many AEFs are based on the destructive superposition of noise and anti-noise signals [2]. Therefore, the anti-noise signal must match the noise signal with opposite sign. Hence, in AEFs the anti-noise signal is determined by the measured noise signal, which is processed by analog or digital circuits.

First analog AEFs are available as integrated circuits [3]. In most analog AEFs, the noise signal is measured and injected for compensation using an operational amplifier circuit. Due to propagation delays, the frequency range of the EMI suppression is limited [4].

In Fig. 1, the suppression of a noise signal, generated by an arbitrary waveform generator emulating the spectrum of a sinusoidal pulse width modulation, with the analog AEF integrated circuit from Texas Instruments [5] is shown. For the case, that the analog AEF is turned off, only the passive components suppress the noise. In the simplified test setup, the harmonic at 200 kHz is reduced by 20 dB and at 4 MHz still a reduction of 15 dB is achieved. Despite of many advantages, there are significant drawbacks of analog filters. Especially worth mentioning are a weak suppression of higher frequencies and difficulties to suppress high power noise. In addition, the design of the filter circuitry is not trivial and instabilities are likely to occur due to the commonly used feed-back structure.

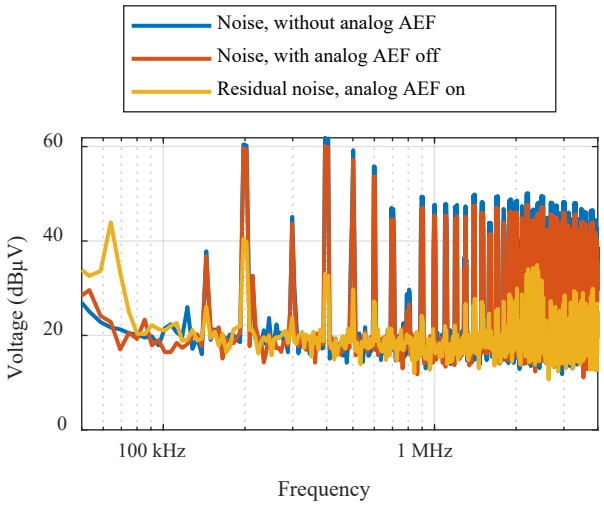


Fig. 1: Measured EMI suppression in a simplified test setup with a commercially available analog AEF

**D**igital **AEF** (DAEF) use digital signal processing with **a**nalog-to-**d**igital **c**onverters (ADC) and **d**igital-to-**a**nalog **c**onverters (DAC) in addition to analog sensing and injection circuits. In [6] the effect of the processing delay on the EMI attenuation was investigated. In an experimental setup it was shown that a processing delay of only 4.5 ns already leads to instability in a feed-back filter. In order to avoid the disadvantage of processing delays, some implementations are based on anti-noise signals predicted from previous values of a

979-8-3503-0735-1/24/$31.00 © 2024 IEEE

periodic noise signal, which allows EMI suppression of high frequency components [7], [8], [9]. This requires a stationary noise-signal as provided by most power electronic systems operated by a PWM control.

**F**ield **p**rogrammable **g**ate **a**rrays (FPGA) in combination with fast ADCs and DACs can be used to achieve the necessary high computing speeds. In [7] adaptive notch filters are used, which are based on the continuous adjustment of the amplitude and phase of a synthesized sinusoidal signal. With the adaptive notch filters, harmonics of a motor drive system are suppressed by up to 27 dB. As discussed in [10], the frequency range of the EMI suppression depends on the available hardware resources of the FPGA. This limits the applicability of practical implementations.

By injecting synthesized and synchronized anti-noise signals, a broadband EMI suppression can be achieved. In [9], the anti-noise signal is calculated with the help of an offline Fast Fourier Transformation. This method requires, besides the periodicity of the noise signal, a strict synchronicity between the noise and anti-noise signal due to the needed calculation time of the anti-noise signal. Here, a very high CM EMI suppression up to 60 dB at 2 MHz and 47 dB at 30 MHz is achieved. However, due to the long signal processing time, fast dynamic changes cannot be handled.

By using an adaptive FIR filter, a broadband CM EMI attenuation in a motor drive system is achieved in [8]. For this purpose, the noise signal is measured and the FIR filter weights are calculated in the FPGA using the Filtered-X **L**east **M**ean **S**quares (LMS) algorithm. A superposition of the logical digital gate control signals is used as the FIR filter's input signal. In addition, the control signals are shortly delayed by 56 ns in order to compensate the processing delay and the time required to inject the anti-noise signal. Therefore, this type of filter is called **d**elayed **d**igital **c**ontrol **DAEF** (DDC-DAEF) in the following. In [8], a noise reduction of 28 dB at 100 kHz, 23 dB at 600 kHz and 6 dB at 10 MHz could be achieved.

In [11], the filter weights are determined by the Wiener-Hopf-equation instead of the Filtered-X LMS algorithm. Therefore, the microprocessor of a **S**ystem-**o**n-**C**hip (SoC) is used to calculate the filter weights, which frees hardware resources in an FPGA. By that, more filter weights can be implemented inside the FPGA than with the FIR filter structure presented in [8]. Thus, the step response of the FIR filter is longer, which is why the achievable noise reduction is increased in a simplified test setup in [11]. This contribution describes a further development of the FIR filter from [8] with the weight calculation described in [11] to increase the CM EMI suppression in a controlled motor drive system.

The paper is organized as follows. First the theory of the FIR filter based DDC-DAEF and methods to determine the FIR filter weights are explained in section II and III, respectively. Then, in section IV the experimental setup for the filter analysis and the hardware implementations for both, a FIR filter based on the Filtered-X LMS algorithm and based on the Wiener-Hopf-equation, are presented. Afterwards, the measurement results are compared for both filter strategies and discussed in section V.

## II. Theory of the FIR filter-based DAEF approach

The used concept for broadband noise cancellation is well-known from discrete-time signal processing [12] and acoustics [13] and is applied for reducing high frequency CM EMI of power electronics in this section. Therefore, the block diagram of the proposed DAEF approach including a FIR filter is presented in Fig. 2. The block diagram is based on discrete-time signal processing methods and therefore also reveals discrete-time signal representations.

At the summation point, the noise signal $d(n)$ destructively interferes with an anti-noise signal $y'(n)$ resulting in the residual noise signal $e(n)$. The variable $n$ denotes the current time index and therefore is a multiple of the sampling time.

Both, the FIR filter $W(z)$ and the primary path $P(z)$, which characterizes the propagation path of the noise signal, are excited by the input signal $x(n)$, which is the superposition of the digital gate control signals [8]. The basic idea is that the FIR filter replicates the noise signal from the input signal. Therefore, the output of the FIR filter $y(n)$ is calculated by the product of a filter weight vector $\boldsymbol{w}$ with the input signal vector $\boldsymbol{x}(n)$:

$$y(n) = \boldsymbol{w}^{\mathrm{T}} \cdot \boldsymbol{x}(n) \tag{1}$$

The input signal vector consists of the last $M + 1$ values of the input signal, where $M$ is the order of the FIR filter. The filter weight vector and input signal vector are defined as follows:

$$\begin{aligned} \boldsymbol{w} &= [w_0, w_1, \dots, w_M]^{\mathrm{T}} \\ \boldsymbol{x}(n) &= [x(n), x(n-1), \dots, x(n-M)]^{\mathrm{T}} \end{aligned} \tag{2}$$

The output of the FIR filter is passed through the so-called secondary (or cancellation) path $S(z)$ resulting in the anti-noise signal $y'(n)$:

$$\begin{aligned} Y'(z) &= S(z) \cdot Y(z) \\ y'(n) &= s(n) * y(n) \end{aligned} \tag{3}$$

Here, $*$ denotes the convolution operator. The secondary path consists of a phase shift and damping respective amplification caused by e.g. ADCs, DACs, the measuring and injecting circuits [8]. The secondary path affects the output signal of the FIR filter before superposition with the noise signal and needs to be considered for stability of the cancellation system [13]. Therefore, a filtered input signal $x'(n)$ is used for the calculation of the filter weights. The filtered input signal results by filtering the input signal with a secondary path estimation analog to equation (3). The resulting residual noise is given by (4).

$$e(n) = d(n) - y'(n). \tag{4}$$

In [8] a detailed description of the model in Fig. 2 is given.

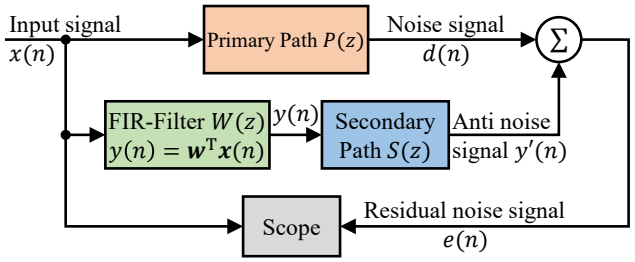


Fig. 2: Block diagram of the FIR-Filter

## III. FIR FILTER ADAPTATION METHODS

In the following, the calculation of the FIR filter weights is described. First, the Wiener-Hopf-equation is presented, which uses the statistics of the input and noise signal to determine linear, optimal filter weights. Then, the Filtered-X LMS algorithm is presented [12].

### A. Wiener-Hopf-equation

The block diagram in Fig. 2 shows that the optimal EMI suppression will be achieved if the transfer function of the FIR filter and secondary path is equal to the transfer function of the primary path: $W(z) \cdot S(z) = P(z)$. Then, the residual noise signal will vanish.

Typically, filters are designed for a desired frequency response. In contrast, the Wiener filter takes a different approach, in which the mean squared error of the residual noise signal is minimized using the discrete-time signals. For this, weak statistical stationarity is assumed for the input and noise signal. Then, the filter weight vector is determined using the Wiener-Hopf-equation, which can be seen as the linear, optimum solution [12]:

$$\boldsymbol{w} = \mathbf{R}^{-1} \cdot \boldsymbol{p} \tag{5}$$

Here, $\mathbf{R}$ is the autocorrelation matrix of the filtered input signal vector and $\boldsymbol{p}$ is the cross-correlation vector of the noise signal and the filtered input signal vector.

### B. Filtered-X LMS algorithm

In practical applications, two problems can lead to reduced EMI suppression when using the Wiener-Hopf-method [12].

First, only a limited number of measured values can be used to calculate the autocorrelation matrix and the cross-correlation vector. As a result, only approximations are available and the calculated filter weights do not correspond to the actual optimum.

Second, the static filter weights cannot react to changes in the EMI signal. The filter weights do not fit any more and the CM EMI suppression is reduced.

With the help of the LMS algorithm [12], [13], which is based as well on the Wiener-Hopf-equation, the above-mentioned problems can be avoided partially by constantly adapting the filter weights. In addition, the LMS algorithm requires relatively few arithmetic operations compared to other adaptation algorithms. With the extension to the Filtered-X LMS algorithm in equation (6), the effects of the secondary path are considered by using the filtered input signal vector $\boldsymbol{x}'(n)$.

$$\boldsymbol{w}(n+1) = \boldsymbol{w}(n) + \mu \boldsymbol{x}'(n) e(n) \tag{6}$$

Here, $\mu$ is the step size of the Filtered-X LMS algorithm. After convergence, the filter weights are optimal in terms of minimizing the mean squared error of the residual noise signal and therefore are equivalent to the solution of the Wiener-Hopf-equation. As the computation resources are limited, the vector lengths are limited too and the LMS algorithm performance can be even lower compared to the Wiener-Hopf-method if the noise is static [11].

## IV. EXPERIMENTAL SETUP

In this section, the implementations for the Filtered-X LMS algorithm and the Wiener-Hopf-equation on the SoC of a Red Pitaya evaluation board are presented. Then, the test setup is shown and described.

### A. Implementation of the DDC-DAEF

The computing speed required to calculate and synthesize the anti-noise signal is high in order to suppress high frequency components of the CM EMI. Therefore, a SoC on a Red Pitaya STEMlab 125-14 Z7020 evaluation board is used. Besides two fast ADCs and DACs with a vertical resolution of 14 bit and a sample rate of 125 MS/s, the evaluation board features a Xilinx Z7020 SoC. This SoC is divided into a programmable logic (FPGA part) and a processing system. Additionally, one ADC of the evaluation board is used to measure the noise signal and both DACs are used to feed the FIR filter's output signal to the injection circuit. The digital gate control signals are read in via **G**eneral **P**urpose **I**nput/**O**utput (GPIO) and then output with a delay of 56 ns ($\Delta t_x$ in Fig. 3).

Also, the FPGA implementation uses a sample rate of 125 MS/s and is used for the calculation of the anti-noise signal. The critical hardware resource are the 220 available DSP48-Blocks, which are used for the multiplication of the input signal vector with the filter weight vector. For the implementation of the Filtered-X LMS algorithm, the filtering of the input signal ($x_{UVW}$ in Fig. 3) with the secondary path estimation and the adaptation of the weights are also realized in the FPGA as shown in Fig. 3 and require DSP48-Blocks [8]. Thus, the number of filter weights is limited to 100 and the microprocessor of the processing system is only used to control the FPGA implementation, e.g. the step size of the Filtered-X LMS algorithm. The FPGA implementation is based on a Simulink model and with help of MATLAB's HDL Coder, a system description in form of Verilog code is generated.

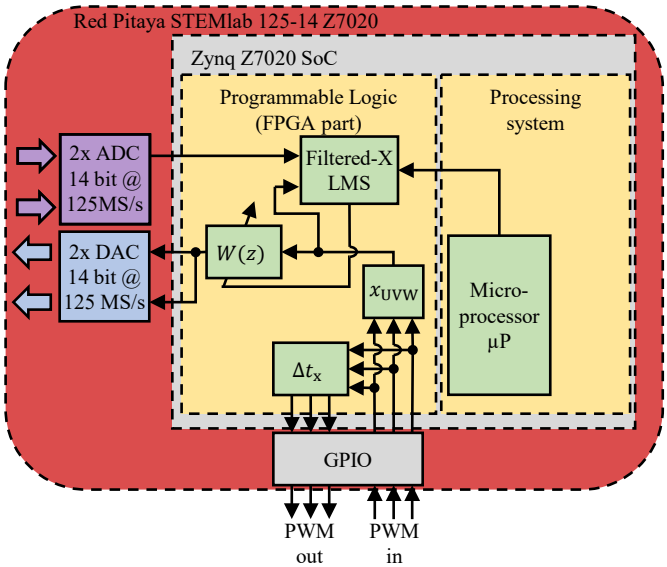


Fig. 3: Block diagram for the implementation of the FIR filter based on the Filtered-X LMS algorithm

The computing speed required to determine the filter weights using the Wiener-Hopf-equation is lower than that required to synthesize the anti-noise signal and is therefore outsourced from the FPGA to the microprocessor. As a result, 200 filter weights are realized in the FPGA to enable a longer step response of the filter. For applying the Wiener-Hopf-equation, the input signal and the noise signal need to be measured. Therefore, the DDR3-Controller in the processing system is used in order to store the signals in the DDR3-RAM at 125 MS/s. The memory access is controlled by the microprocessor. The input signal is filtered with the secondary path estimation inside the microprocessor and additionally, an eighth order low pass filter with a cutoff frequency of 25 MHz is used to filter out high frequency noise in the measured data. After calculating the filter weights with the Wiener-Hopf-equation, these are transferred to the FPGA implementation. The block diagram for the implementation is shown in Fig. 4.

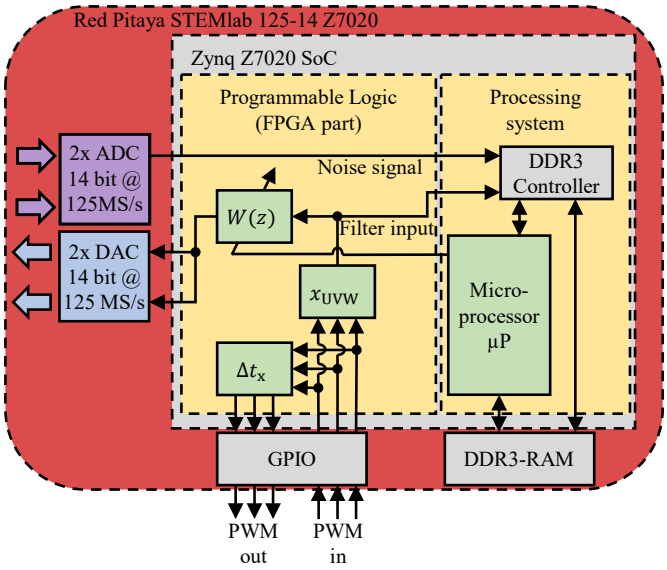


Fig. 4: Block diagram for the implementation of the FIR filter based on the Wiener-Hopf-equation

## B. *Motor inverter setup for DDC-DAEF performance evaluation*

The schematic of the test setup is depicted in Fig. 5, while Fig. 6 shows the major part of the test setup.

The test setup is powered by an isolated DC voltage source with 48 V. The motor inverter essentially consists of three GaN half bridges with a switching frequency of 100 kHz. The digital gate control signals are generated by a field-oriented motor control algorithm running within a separate FPGA [10], which is referred to as motor control board in the following.

The main part of the cancellation system is the Red Pitaya board running the filter algorithm (AEF-Red Pitaya). The disturbance on each DC line is measured with two **a**rtificial **n**etworks (ANs) and the CM EMI signal is extracted via a Common Mode / Differential Mode Switch (CMDM8700 from Schwarzbeck). Then, the CM EMI signal is attenuated by 20 dB such that the input voltage range (±1V) of the ADC is not exceeded. A power splitter is used to transmit the noise signal to the EMI test receiver (R&S ESRP, RBW = 9 kHz, receiver mode, 20 ms measurement time) and to the AEF-Red Pitaya. To match impedances, a 50 Ω termination is in parallel to the ADC. As described in section II, the AEF Red Pitaya also needs the digital gate control signals from the motor control board to calculate the filter weights. To compensate the time required for synthesis and injection of the anti-noise signal, the digital gate control signals are slightly delayed by 56 ns in the AEF Red Pitaya. By delaying the digital gate control signals, the main limitation of analog feedforward AEF (time delay while feeding forward a measured EMI signal) is bypassed. The output signal of the FIR filter is fed to two amplifiers (ADA4870 ARR-EBZ from Analog Devices) via the two fast DACs of the AEF Red Pitaya and injected onto both DC lines with 22 nF capacitors. The CM input impedance of the motor inverter is increased by a ferrite (74272722 from Würth Elektronik) such that the injected cancellation current flows to the ANs.

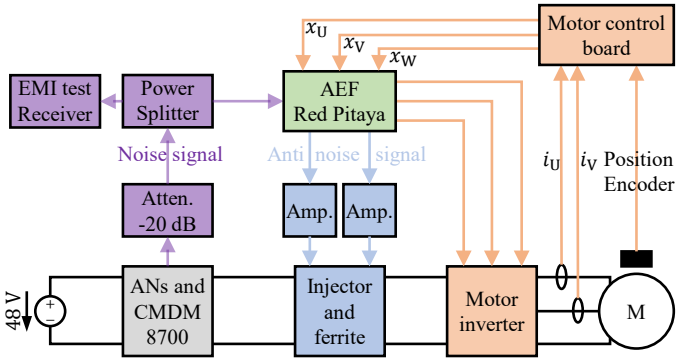


Fig. 5: Schematic of the test setup

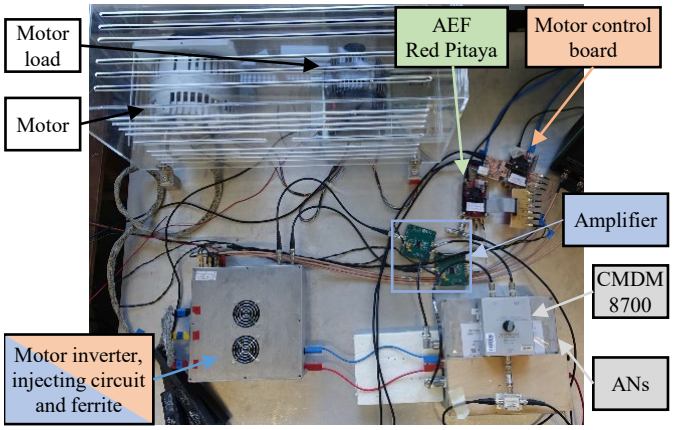


Fig. 6: Picture of the main part of the test setup

## V. Measurement Results and Discussion

In the following, the achieved CM EMI suppression with the DDC-DAEF is compared for both weight calculation techniques (Filtered-X LMS algorithm with 100 weights [8] and the Wiener-Hopf-equation with 200 weights). In addition, the results are discussed for a mechanically loaded motor and a freewheeling motor. Afterwards, a modification of the filter

weights' calculation based on the Wiener-Hopf-equation is explained in order to achieve a higher CM EMI reduction.

### A. CM EMI reduction with mechanically loaded motor

In the following, the achieved CM EMI suppression of the presented DDC-DAEF approach for the mechanically loaded motor is investigated. The setpoint for the electrical frequency on the AC side is 20 Hz.

The noise and residual noise with mechanically loaded motor are shown in Fig. 7. With both weight calculation techniques, a similar CM EMI suppression up to ≈15 MHz is achieved. Only in the frequency range between 500 kHz and 3 MHz the CM EMI reduction with the Wiener-Hopf-equation is up to 10 dB larger and the harmonics at 500 kHz and at 2 MHz are reduced by ≈23 dB. The larger CM EMI reduction with the Wiener-Hopf-equation can be explained by the increased number of filter weights and the associated longer step response of the FIR filter. As presented in [11], the longer step response of the FIR filter with 200 weights is equivalent to a longer anti-noise signal, which leads to an increased CM EMI attenuation. At the switching frequency of 100 kHz, the noise is suppressed by ≈20 dB. The noise reduction at 10 MHz is about 6 dB.

In the frequency range between 3 MHz and 8 MHz, the CM EMI suppression with the Filtered-X LMS algorithm is up to 5 dB higher. This could be due to inaccuracies in the secondary path estimation. These are partly compensated by the constant adaptation with a small step size in the Filtered-X LMS algorithm. For higher frequencies, errors in the time delay have a greater influence on the phase error, which is why the adaptation can no longer compensate for the error in the secondary path estimation and the curves for the Wiener-Hopf-equation and the Filtered-X LMS algorithm are almost similar.

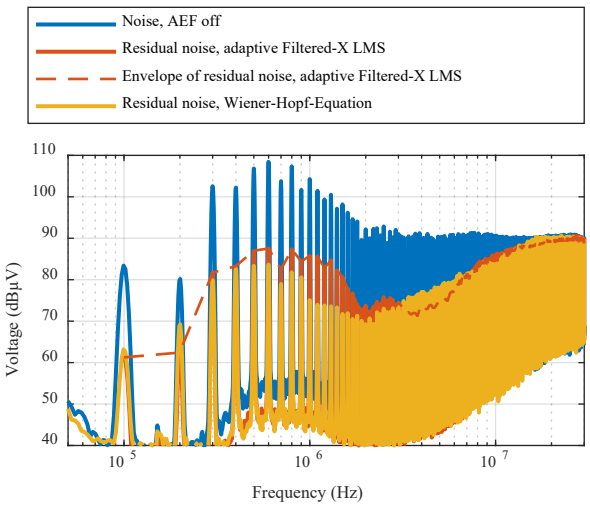


Fig. 7: CM EMI suppression with the FIR filter with a mechanically loaded motor

### B. CM EMI reduction with freewheeling motor

In addition, the CM EMI suppression with a freewheeling motor is investigated. Again, the setpoint for the electrical frequency on the AC side is 20 Hz. The power provided by the DC source is now 30 W instead of 150 W with the mechanically loaded motor.

The noise for the AEF turned off with a freewheeling motor and the residual noise with both weight calculation techniques are shown in Fig. 8. Like the investigation with a mechanically loaded motor, here the noise is suppressed over a wide frequency range up to ≈15 MHz. Again, in the frequency range between 300 kHz and 3 MHz, the CM EMI reduction with the Wiener-Hopf-equation and 200 filter weights is up to 10 dB greater. The CM EMI reduction with the Wiener-Hopf-equation for the harmonic at 500 kHz is ≈25 dB and at 2 MHz about 26 dB. At 10 MHz the noise is still reduced by about 7 dB with both weight calculation techniques. However, at 20 MHz and 30 MHz an amplification of the noise by using the Wiener-Hopf-equation of about 3 dB is visible. Again, in the frequency range between 3 MHz and 8 MHz, the CM EMI suppression with the Filtered-X LMS algorithm is higher.

There is no significant difference in the CM EMI reduction for the case with a mechanically loaded motor and for the case with a freewheeling motor. Therefore, for the sake of simplicity, the following investigation is carried out with a freewheeling motor.

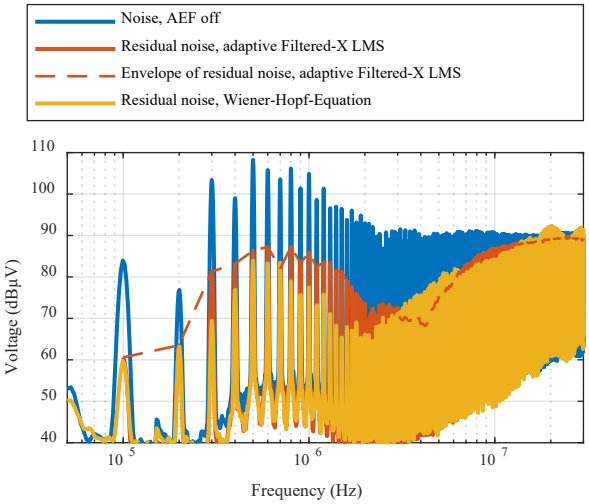


Fig. 8: CM EMI suppression with the FIR filter with freewheeling motor

As already mentioned, small errors in the secondary path estimation and the approximation of the autocorrelation matrix and cross-correlation vector can lead to a reduced CM EMI suppression when using the Wiener-Hopf-equation. In order to improve the CM EMI suppression, an iterative optimization of the filter weights, similar to the LMS algorithm in (6), is performed:

$$\boldsymbol{w}(n+1) = \boldsymbol{w}(n) + \alpha \cdot \boldsymbol{R}(n)^{-1} \cdot \boldsymbol{p}(n) \qquad (7)$$

Here, $\alpha$ is a weighting factor for the new calculated filter weights. In Fig. 9 the CM EMI suppression for the test setup with a freewheeling motor is shown for $\alpha = 0.1$ and 30 iterations. Generally, a higher CM EMI suppression with the iterative calculation of the filter weights using the Wiener-Hopf-equation can be seen. The result is compared to the FIR filter based on the Filtered-X LMS algorithm and to the Wiener-

Hopf-approach without iterative optimization. The attenuation performance is summarized in Table 1. With the iterative calculation, the CM EMI reduction is about 33 dB at 100 kHz and still 15 dB at 10 MHz. At 2 MHz, the CM EMI attenuation is slightly reduced by 2 dB with the iterative approach.

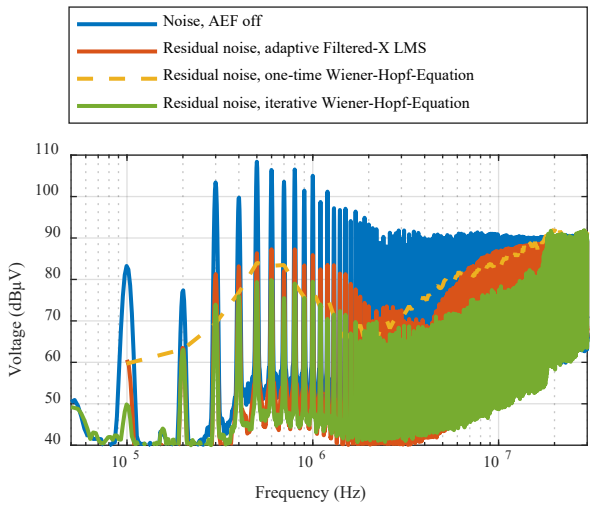


Fig. 9: CM EMI suppression with the FIR filter with freewheeling motor and different adaptation methods

Table 1: Comparison of the achieved CM EMI attenuation for the presented adaptation methods and different filter lengths

| Frequency | Filtered-X LMS algorithm and 100 filter weights | One-time Wiener-Hopf-equation and 200 filter weights | Iterative Wiener-Hopf-equation and 200 filter weights |
|---|---|---|---|
| 100 kHz | 23 dB | 24 dB | 33 dB |
| 500 kHz | 22 dB | 25 dB | 29 dB |
| 2 MHz | 20 dB | 26 dB | 24 dB |
| 10 MHz | 4 dB | 5 dB | 15 dB |

## VI. Conclusion

This paper describes a further development of a DDC-DAEF based on a FIR filter. Here, the filter weights are calculated using the Wiener-Hopf-equation. The digital gate control signals are delayed by 56 ns to compensate the time required to calculate and inject the anti-noise signal. In contrast to a Filtered-X LMS-based FIR filter implemented completely in an FPGA, the FIR filter based on the Wiener-Hopf-method calculates the filter weights outside the FPGA in a microprocessor on the same SoC to save FPGA resources. This allows to increase the number of implementable FIR filter weights. By iteratively calculating the filter weights the noise reduction is increased. In an inverter-motor setup, 33 dB at 100 kHz, 29 dB at 500 kHz and still 15 dB at 10 MHz could be reached. Due to the iterative calculation of the filter weights, changing EMI signals can be handled.

In further work, the iterative calculation of the filter weights could be improved further, the usage of the SoC architecture can be optimized, and dynamic changes of, e.g., the engine speed or load are to be investigated.

## Acknowledgement

The work in this paper was funded by the Federal Ministry for Economic Affairs and Climate Action as part of the project Power2EMC (Intelligent, EMC-Compliant and Energy Efficient Control of Power Electronic Systems) with reference number 19I23005G. The responsibility for this publication is held by the authors only.

## References

[1] K. Mainali und R. Oruganti, „Conducted EMI Mitigation Techniques for Switch-Mode Power Converters: A Survey“, *IEEE Trans. Power Electron.*, Bd. 25, Nr. 9, S. 2344–2356, Sep. 2010.

[2] B. Narayanasamy und F. Luo, „A Survey of Active EMI Filters for Conducted EMI Noise Reduction in Power Electronic Converters“, *IEEE Trans. Electromagn. Compat.*, Bd. 61, Nr. 6, S. 2040–2049, Dez. 2019, doi: 10.1109/TEMC.2019.2953055.

[3] A. Kumar, Y. Hou, Y. Ramadass, T. Merkin, T. Hegarty, und A. Obidat, „An Active EMI Filter for High-Power Off-Line Applications“, in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, USA: IEEE, März 2023, S. 2063–2067. doi: 10.1109/APEC43580.2023.10131427.

[4] Y. Zhang und D. Jiang, „An Active EMI Filter in Grounding Circuit for DC Side CM EMI Suppression in Motor Drive System“, *IEEE Trans. Power Electron.*, Bd. 37, Nr. 3, S. 2983–2992, März 2022, doi: 10.1109/TPEL.2021.3110144.

[5] „TPSF12C3-Q1 three-phase active EMI filter evaluation board“. [Online]. Verfügbar unter: https://www.ti.com/tool/TPSF12C3QEVM

[6] J. Ji, W. Chen, X. Yang, und J. Lu, „Delay and Decoupling Analysis of a Digital Active EMI Filter Used in Arc Welding Inverter“, *IEEE Trans. Power Electron.*, Bd. 33, Nr. 8, S. 6710–6722, Aug. 2018, doi: 10.1109/TPEL.2017.2758682.

[7] T. Dorlemann, A. Bendicks, und S. Frei, „FPGA-based Adaptive Notch Filters for the Active Cancellation of Varying Electromagnetic Emissions of Power Electronic Inverter Systems“, in *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, Raleigh, NC, USA: IEEE, Juli 2021, S. 307–312. doi: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559297.

[8] J. Aigner, M. Lemke, T. Dörlemann, und S. Frei, „Broadband Active Common Mode EMI Suppression of Motor Inverters with Adaptive FIR Filters Using Delay-Compensated Digital Gate Control Signals“, *Preprint available at https://bs.etit.tu-dortmund.de/publikationen/.*

[9] A. Bendicks, M. Gerten, und S. Frei, „Active Cancellation of Periodic CM EMI at the Input of a Motor Inverter by Injecting Synthesized and Synchronized Signals ($S^3$-AEF)“, *IEEE Trans. Power Electron.*, Bd. 37, Nr. 10, S. 11951–11961, Okt. 2022, doi: 10.1109/TPEL.2022.3172205.

[10] M. Lemke, T. Dörlemann, und S. Frei, „FPGA Based Motor Inverter Control for Strictly Synchronous Digital Active EMI Cancellation“, in *2023 International Symposium on Electromagnetic Compatibility – EMC Europe*, Krakow, Poland: IEEE, Sep. 2023, S. 1–6. doi: 10.1109/EMCEurope57790.2023.10274249.

[11] M. Lemke, T. Dörlemann, J. Aigner, und S. Frei, „Analyse der FIR-Filterlänge zur breitbandigen aktiven Störunterdrückung in leistungselektronischen Systemen“, gehalten auf der EMV Köln, Köln, 2024.

[12] B. Widrow und S. D. Stearns, *Adaptive signal processing*. in Prentice-Hall signal processing series. Englewood Cliffs, N.J: Prentice-Hall, 1985.

[13] S. M. Kuo und D. R. Morgan, „Active noise control: a tutorial review“, *Proc. IEEE*, Bd. 87, Nr. 6, S. 943–975, Juni 1999.