Application of Levenberg-Marquardt Method for Optimizing Gate Driving Signals of a DC/DC Converter to Reduce Switching Resonances

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***Abstract* — In power electronic systems often serious electromagnetic emissions are caused by the fast switching power transistors. RF oscillations may be triggered by the switching events and parasitic capacitances and inductances. In the frequency spectrum a narrowband peak can be seen. A common countermeasure is to decrease the switching slopes steepness of the gate drive signal by, e.g., inserting an additional gate resistor. This leads to decreased disturbances but also to a reduced efficiency of the system. Optimized gate control signals can improve the electromagnetic compatibility without seriously affecting the system efficiency. In this paper, a target signal-oriented gate control is applied to reduce narrow-band disturbances while maintaining fast switching slopes. The gate drive signal is optimized in the frequency domain by the Levenberg-Marquardt method. The approach is applied to a DC/DC boost converter in simulation and a laboratory setup. The benefits of the proposed method regarding to the reduction of electromagnetic disturbances and maintaining a high system efficiency are discussed.**

***Keywords* — active gate drivers, power electronics, GaN-HEMT, nonlinear optimization.**

I. Introduction

Power electronic converters based on power transistors are a key component for energy conversion and energy distribution. In modern converters, wide-bandgap semiconductors such as gallium nitride (GaN) or silicon carbide (SiC) transistors are used. Steeper switching edges can be achieved with the advantage of reduced switching losses compared to conventional silicon MOSFETs. The disadvantage, however, is that the fast switching processes cause broadband noise and often significant resonances [1]. As an example, a DC/DC boost converter, as shown in Fig. 1, is considered. The use of a conventional gate driver (CGD) with an approximately trapezoidal-shaped gate drive signal results in high frequency attenuated oscillations at the switching node (SN) of the converter after the switching operations which result in a peak in the spectrum. This is due to the parasitic reactive elements, which are shown in gray in Fig. 1. The oscillation in the turned-off state of the transistor is caused by the resonant circuit consisting of the parasitic drain-source capacitance C_{ds} of the transistor, the diode with its parasitic capacitance C_{d}, the parasitic inductance L_{para}, typically caused by the PCB layout, and the parallel circuit consisting of the output capacitance C_{out} and the load resistor R_{L}.

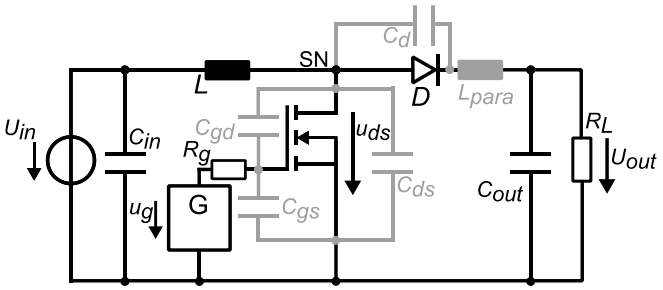

Fig. 1: Equivalent circuit of a DC/DC boost converter with parasitic elements (grey)

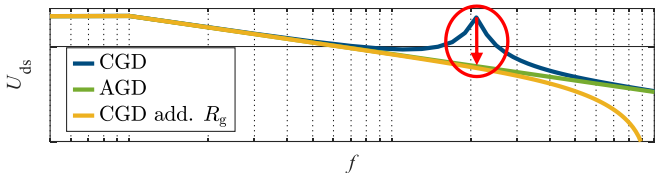

Fig. 2: Schematic illustration of the drain-source voltage in the frequency domain using a CGD, an AGD or a CGD with an additional gate resistor

A simple approach to reduce the oscillations is to use an additional gate resistor, R_{g} in Fig. 1. This reduces the steepness of the switching slopes, and the resonance can be lower. On the other hand, the switching losses are highly increased by the slower switching processes. An active gate driver (AGD) can provide improved control signals. Arbitrary waveform generator-based drivers can provide almost arbitrary gate signals and control the EMI spectrum. Exemplarily spectra of the different configurations are shown in Fig. 2

In this paper it is assumed that only the resonance peak is to be reduced by an appropriate AGD voltage $u_{\mathrm{g}}(t)$ which influences the rising slope and thus the efficiency of the transistor as little as possible. As the transfer characteristic between u_{g} and u_{ds} is highly nonlinear this is a challenging task.

The here applied approach for active gate driving is shown in Fig. 3. Essentially, the setup can be divided into two parts. One is the analog part with the gate driving circuit and the voltage sensing and the other is a digital part containing the control unit with an optimizer and signal processing. Different approaches for analog active gate drivers are known. Often, as described in [2] and [3], variable voltage sources, variable current sources or networks of variable resistors are used. In this work,

a variable voltage source is used as the gate driving circuit to apply the signals that are calculated in the control unit to the gate of the transistor.

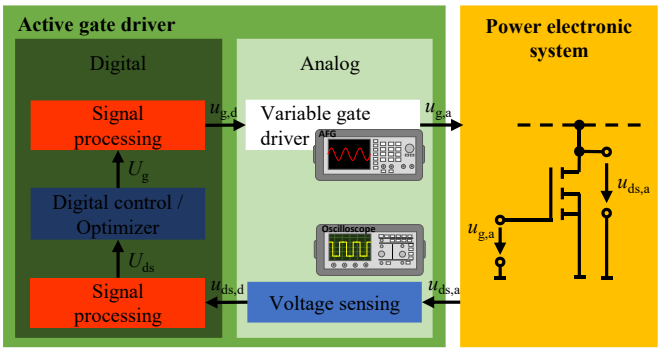

Fig. 3: General schematic of an active gate driver

The gate signal is determined in the digital control unit based on the drain-source voltage. Different approaches are known. In [4] the gate drive signal is determined based on the output characteristic of the transistor and in [5] based on the switching characteristics of the transistor. However, in order to realize a good active gate control with these approaches, a very high accuracy of the models is required, which is very difficult to realize. Other approaches that do not require models of the system are based on optimization algorithms. Heuristic optimization algorithms are used in [6], [7] and [8]. However, the disadvantage of heuristic methods is that they have a relatively slow convergence rate and the results are not necessarily reproducible. A more promising approach is the use of deterministic optimization methods. A pattern search algorithm is used in [9] and a Newton's method with a stepwise adaptation of the objective function is presented in [10]. This method has the disadvantage that the objective function must specify a value for each harmonic of the gate drive signal that should be optimized. Due to the nonlinear transfer characteristic and the signal for reliable function of the considered circuit, the range of the drain-source voltage is limited. However, determining suitable values so that a physical target signal is obtained proves to be very difficult in practice. The problem is discussed in more detail in [11].

To reduce the mentioned optimization problems, here the Levenberg-Marquardt method (LMM) of [12], a modification of the Newton's method, is used to iteratively optimize the gate drive signal. A single resonance peak in the spectrum of the drain-source voltage should be reduced by an optimized gate drive signal. The LMM is used with a scalar objective function whose minimum is sought. In order to achieve convergence, there is no need for a physical target signal as in [10]. The method is also more robust regarding the choice of initial values.

The theory of optimizing the drain-source voltage based on the LMM in the frequency domain is explained in section II. In section III, the method is applied to a DC/DC boost converter. Moreover, the trade-off between EMC and efficiency is considered. Furthermore, the influence of optimization parameters on the optimization result and the efficiency of the optimization is analyzed and discussed. Section IV summarizes the results and presents possible extensions to the method.

II. AGD WITH LEVENBERG-MARQUARDT METHOD IN THE FREQUENCY DOMAIN

The proposed method for controlling the gate is described below. The signal of the drain-source voltage of a power transistor is controlled by optimizing the signal of the associated gate drive voltage.

A. Optimization in the Frequency Domain

As mentioned before, the disturbance of the drain-source voltage to be reduced is considered as narrow-banded. The transistor is driven by a stationary pulse width modulated (PWM) signal and the resulting drain-source voltage is considered in the steady state. Therefore, the time domain-signals can be represented by a Fourier-series. Here, the complex representation of the Fourier-series, given in equation (1) for the general voltage u in dependence of the time t, is considered:

$$u(t) = \sum_{k=-N}^{N} \left(U_{k,\mathrm{Re}} + j \cdot U_{k,\mathrm{Im}}\right) \cdot e^{j2\pi f_0 k t}. \tag{1}$$

In the following, all time domain signals are represented in lowercase letters and the corresponding Fourier-series coefficients in capital letters. The real and imaginary part $U_{k,\mathrm{Re}}$ and $U_{k,\mathrm{Im}}$ for the k-th element of the two-sided complex spectrum of the Fourier-series are determined by a fast Fourier transformation (FFT). In this case, N harmonics with a fundamental frequency of f_0 are observed. Only the positive coefficients of the Fourier-series are considered in the optimization due to the symmetry of the Fourier-series coefficients for positive and negative k. The negative coefficients are considered by transforming back to the time domain accordingly. The transformation from the frequency to the time domain is done using an inverse Fourier transformation (IFFT).

B. Determination of the Target Signal

As described before, the LMM is used to solve a minimization problem. Here, the target is the reduction of the electromagnetic disturbances caused by the triggered oscillation after the switching events. This is done by reducing the harmonic which is the highest in the peak in the spectrum of the drain-source voltage shown in Fig. 4 with the red cycle. This harmonic corresponds to the fundamental frequency of the attenuated oscillation in the time domain signal. Due to the attenuation of the oscillation, there is not only the harmonic of the fundamental frequency increased, but also a narrowband range around this frequency. But if the harmonic with the fundamental frequency is decreased, also the other harmonics of the peak are reduced. So, only this harmonic with the frequency m is considered in the objective function F shown in equation (2):

$$F = \left(U_{\mathrm{ds,Opt,m}} - U_{\mathrm{ds,t,m}}\right)^2. \tag{2}$$

The square of the difference between the actual value $U_{\mathrm{ds,Opt,m}}$ of the m-th harmonic and the target value $U_{\mathrm{ds,t,m}}$ for the m-th harmonic is determined. The target value is the lower limit of this harmonic of U_{ds}, because the amplitude could not be minimized to zero. This is caused by the signal for reliable function of the drain-source voltage. The signal without disturb-

ances has a finite value at the harmonic to be optimized. Otherwise, the minimization problem could not be solved with the desired maximum error, because with this target no physical signal can be generated. In this case, the LMM converges to the possible minimum, but the desired maximum error will not be reached.

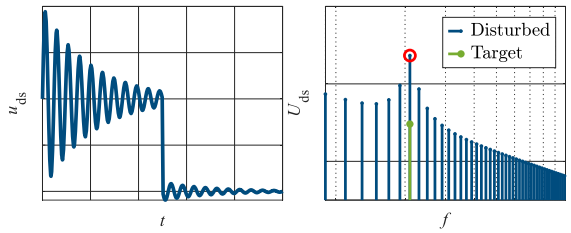

Fig. 4: Disturbed time domain signal (left) and frequency domain signal with target resonance amplitude (right)

C. Levenberg-Marquardt Method in the Frequency Domain

In the following, the LMM for active gate driving applied to frequency domain data is explained. The approach is schematically illustrated in Fig. 5 by a flowchart. To solve a minimization problem using the LMM, it is necessary to have an objective function which is the sum of squares. The objective function given in equation (2) contains only one sum term. The iteration rule,

$$\mathrm{U}_\mathrm{g}^{(\mathrm{n}+1)} = \mathrm{U}_\mathrm{g}^{(\mathrm{n})} - \left(\tilde{\mathbf{H}}^{(\mathrm{n})} + \mu^{(\mathrm{n})} \cdot \mathbf{E}\right)^{-1} \cdot \mathrm{G}^{(\mathrm{n})} \cdot F^{(\mathrm{n})}, \tag{3}$$

is used to optimize the harmonics of the gate drive voltage to reach this target. The harmonics to be optimized of the gate drive signal in iteration step $\mathrm{n}+1$ are determined depending on the corresponding harmonics in the iteration step n, a scaling factor $\mu^{(\mathrm{n})}$, the unit matrix $\mathbf{E}$, the objective function $F^{(\mathrm{n})}$, the gradient $G^{(\mathrm{n})}$ and the approximation of the Hessian $\tilde{\mathbf{H}}^{(\mathrm{n})}$. Each value depends on the gate drive signal in iteration step n. As it is not possible to model the entire power electronic circuit in a sufficient way and to solve the resulting nonlinear differential equations analytically, also the Hessian cannot be determined analytically. The computational effort is very high. Therefore, the approximated Hessian,

$$\tilde{\mathbf{H}}^{(\mathrm{n})} = \mathrm{G}^{(\mathrm{n})} \cdot \mathrm{G}^{(\mathrm{n})^T}, \tag{4}$$

is used. The gradient and the transposed gradient are multiplied. The gradient for the objective function with respect to the real and imaginary part of the K harmonics of the gate drive signal to be optimized is here determined by the following equation,

$$\mathrm{G}^{(\mathrm{n})} = \left[\frac{\partial F^{(\mathrm{n})}}{\partial U_{\mathrm{g,1,Re}}^{(\mathrm{n})}} \quad \frac{\partial F^{(\mathrm{n})}}{\partial U_{\mathrm{g,1,Im}}^{(\mathrm{n})}} \quad \cdots \quad \frac{\partial F^{(\mathrm{n})}}{\partial U_{\mathrm{g,K,Re}}^{(\mathrm{n})}} \quad \frac{\partial F^{(\mathrm{n})}}{\partial U_{\mathrm{g,K,Im}}^{(\mathrm{n})}}\right], \tag{5}$$

where each derivative is determined by central differences to get a high accuracy of the gradient. Furthermore, the Hessian $\tilde{\mathbf{H}}^{(\mathrm{n})}$ can become singular. Then, the inverse Hessian cannot be determined. For this reason, the scaling factor $\mu^{(\mathrm{n})}$ is inserted. Due to the addition of $\mu^{(\mathrm{n})}$ to the diagonal elements of $\tilde{\mathbf{H}}^{(\mathrm{n})}$ it can be reached that the resulting matrix is always regular and semi-definite. This way the inverse of the matrix can be determined, and the solution converges to a minimum of the objective function. If the value of the objective function in iteration step n is decreased, the scaling factor $\mu^{(\mathrm{n})}$ is also decreased by the division by the parameter ψ. Otherwise, $\mu^{(\mathrm{n})}$ is increased by a multiplication with ψ and the gradient of the previously best solution is used in equations (3) and (4). If $\mu^{(\mathrm{n})}$ has a high value, the method approaches the Gauß-Newton method, as described in [12]:

$$\mathrm{U}_\mathrm{g}^{(\mathrm{n}+1)} = \mathrm{U}_\mathrm{g}^{(\mathrm{n})} - \frac{1}{\mu^{(\mathrm{n})}} \cdot \mathrm{G}^{(\mathrm{n})} \cdot F^{(\mathrm{n})}. \tag{6}$$

Otherwise, if the value of $\mu^{(\mathrm{n})}$ is small, the method approaches Newton's method,

$$\mathrm{U}_\mathrm{g}^{(\mathrm{n}+1)} = \mathrm{U}_\mathrm{g}^{(\mathrm{n})} - \tilde{\mathbf{H}}^{(\mathrm{n})^{-1}} \cdot \mathrm{G}^{(\mathrm{n})} \cdot F^{(\mathrm{n})}. \tag{7}$$

To terminate the optimization process, a termination condition is required. As shown in Fig. 5, the objective function is compared to the upper accepted limit of the error ε.

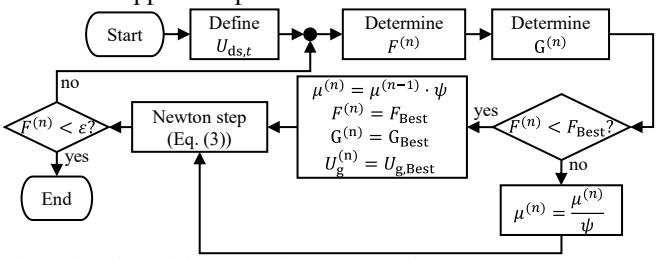

Fig. 5: Flowchart of the proposed AGD approach

III. Application of the AGD-Approach to a DC/DC Boost Converter

In the following, the proposed active gate driving approach is applied to a DC/DC boost converter in simulations and in a laboratory test setup. Different optimization parameters are considered. Furthermore, this AGD method is compared to the described conventional method of reducing the steepness of the switching slopes and the trade-off between EMC and efficiency is analyzed.

A. Simulation Model and Laboratory Setup

A DC/DC boost converter, as shown in Fig. 6, is considered. The low-side transistor is switched with a fundamental fre-

Table 1: Used components and equipment in simulation and the laboratory setup

Components			
GaN-HEMT	EPC2020	Efficient Power Conversion	
Amplifier	EVAL-ADA4870	Analog Devices	
Parameter	Value	Parameter	Value
Uin in V	12	Cin in µF	10
Rg in Ω	5	Cout in µF	12
RL in Ω	25	L in µH	3.25
Equipment			
Oscilloscope	HDO6104A	Teledyne LeCroy	
Arbitrary function generator	AFG31152	Tektronix	
Temperature data logger	TC-08	Pico Technology	

quency of 1 MHz and a duty cycle of 50 %. A GaN HEMT EPC2020 is used with the specifications of the datasheet in [13] and of the LTspice model of [14]. In the simulation a high-side diode with parasitic capacitance is used. In the laboratory setup, the transistor in reverse conduction mode is used instead of the diode. In the simulation an inductance of 20 nH is assumed to model the parasitic layout inductance. A photo of the laboratory setup is shown in Fig. 7. To evaluate the efficiency in the laboratory setup, the temperature of the switched transistor is measured with a type K-type thermocouple and a temperature data logger. The parameter setup, used equipment and components are shown in Table 1.

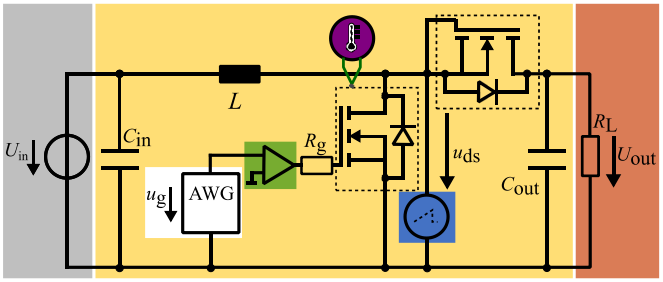

Fig. 6: Equivalent circuit of the considered DC/DC boost converter

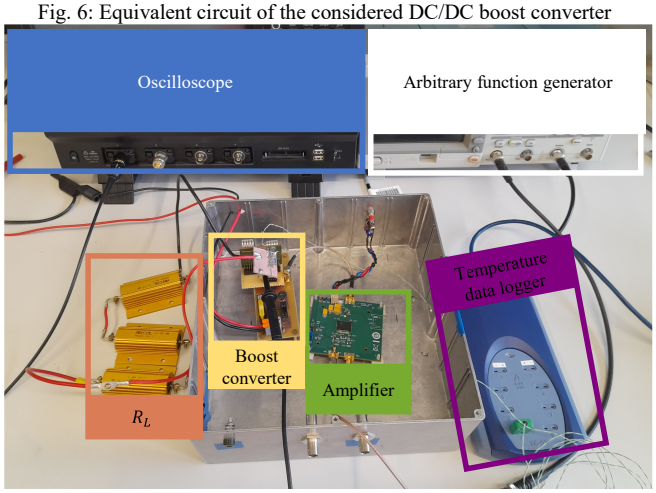

Fig. 7: Photo of the laboratory setup with the DC/DC boost converter

B. Application of the AGD Approach in the Simulation

The proposed AGD optimization approach is applied to reduce the oscillations after the switching events of the drain-source voltage. At first a conventional gate drive signal, in this case a trapezoidal signal with a duty cycle of 50 % as shown in Fig. 8 in blue, is applied to define the target $U_{\mathrm{ds,t,m}}$ of equation (2). The disturbed drain-source voltage of Fig. 9 results. An attenuated oscillation can be observed after the transistor is switched off. The resulting peak in the spectrum can be seen on the right in this figure. The maximum amplitude in the peak occurs at 35 MHz. This is the harmonic to be decreased by 15 dB. The amplitude of $U_{\mathrm{ds,t,35MHz}}$ becomes 115 dBµV which is marked by the yellow dot in Fig. 9 on the right. To reach this target, the entire spectrum of the gate drive signal is optimized using the iteration rule of equation (3). The scaling factor $\mu^{(0)}$ is chosen to 30 at the beginning of the optimization and ψ is set to 10. The computation effort of the optimization is very high due to the necessary high sampling rate, because of the steep switching slopes, which correlates to the number of considered harmonics. In this case, 10 001 coefficients of the Fourier-series are optimized. The termination condition is fulfilled if the objective function is smaller then $\varepsilon = 10^{-6}$. The maximum number of iterations is set to 20. After the optimization, the green gate drive signal in Fig. 8 results which leads to the drain-source voltage in Fig. 9, also in green. The target is reached after 13 iterations and the maximum overshoot decreases from 36.1 V to 27.4 V.

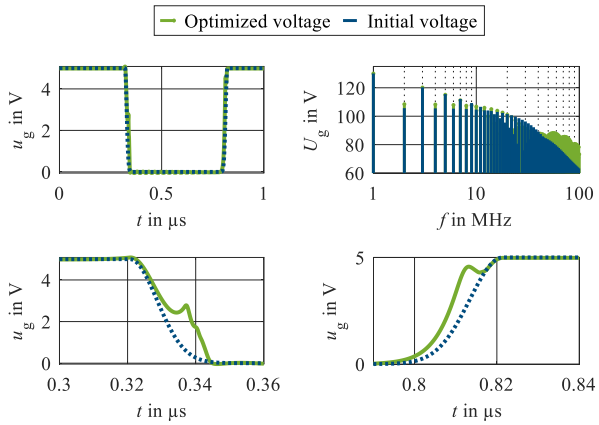

Fig. 8: Initial value and optimized gate drive voltages of the simulation setup in the time and the frequency domain and zoom of the switching slopes of u_g (bottom)

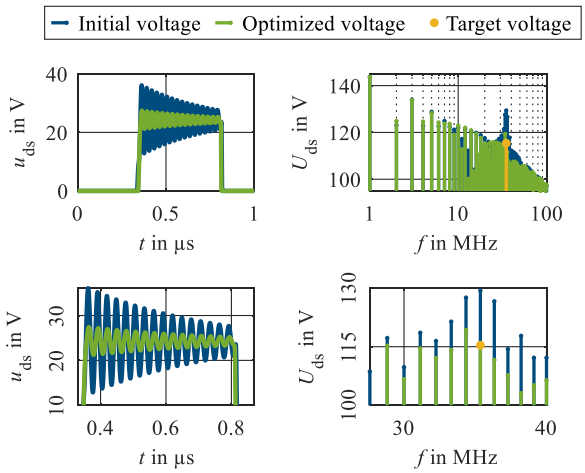

Fig. 9: Simulated disturbed, optimized and target drain-source voltage in the time (left) and the frequency domain (right) with zoom to the disturbances (bottom)

C. Application of the AGD Approach in the Laboratory Setup

In this section, the optimization approach is applied in the described laboratory setup. In section III.B, the entire spectrum of the gate drive signal is optimized. This is not feasible in the laboratory setup. The computation of the gradient cannot be done with an acceptable amount of time. Therefore, less harmonics of U_g are optimized. The usability of this approach is shown in the simulation in [15]. Here, the real and imaginary part of the coefficients of the Fourier-series of U_g at 23 MHz is optimized. If only single harmonics are optimized, oscillations occur in the gate drive signal in the on and off state, which only have a negligible effect to the drain-source voltage due to the

highly nonlinear transfer characteristic of the power transistor. Only the power losses in the on and off state are increased. To avoid this, the oscillations are cut off in the on and off state. Therefore, further harmonics of U_g are changed as illustrated in Fig. 10 in the spectrum.

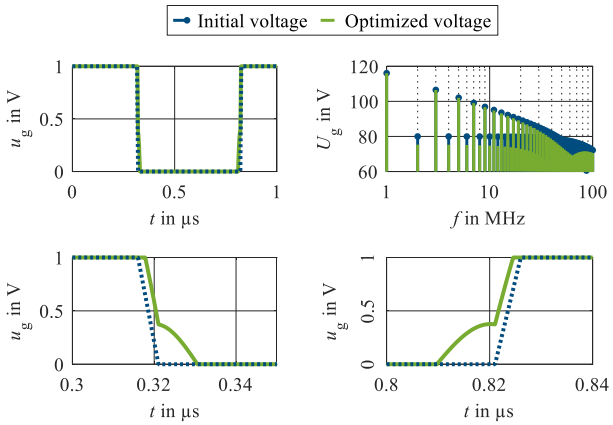

Fig. 10: Initial value and optimized gate drive voltages of the measurement setup in the time and the frequency domain (top) with zoom of the switching slopes of u_g (bottom)

Applying the trapezoidal gate drive signal of Fig. 10 in blue, the blue initial drain-source voltage in Fig. 11 results in the laboratory setup. The disturbance occurs at 30 MHz and must be reduced by 15 dB, as shown by the yellow line. The scaling factor $\mu^{(0)}$ and the parameter ψ are also set to 30 and 10 respectively. The upper accepted limit of the termination condition is set to $\varepsilon = 10^{-6}$ and the maximum number of iteration steps is limited to 20. After the optimization, the green gate drive signal in Fig. 10 and drain-source voltage in Fig. 11 results. The target reduction is sufficiently fulfilled and the maximum overshoot of u_{ds} is reduced from 29.3 V to 25.9 V.

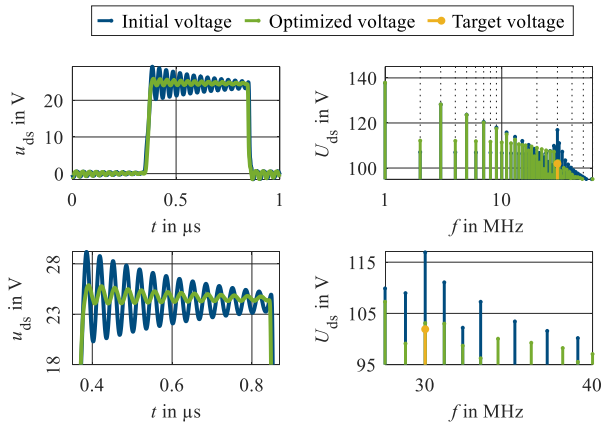

Fig. 11: Measured disturbed, optimized and target drain-source voltage in the time and the frequency domain (top) and zoom to the disturbances (bottom)

D. Comparison to a Gate Resistor Slope Control

In this section, the proposed AGD approach is compared to an additional gate resistor for slope control. In this case the initial point is the same as for the AGD approach. A trapezoidal signal with a duty cycle of 50 %, a rise and fall time of 5 ns and a fundamental frequency of 1 MHz is applied to the gate of the power transistor in the laboratory setup. Based on this, the rise and fall times of the trapezoidal gate drive signal are increased up to 80 ns as marked in Fig. 12. To evaluate the trade-off between the EMC and the efficiency of the system, in Fig. 12 the maximum overshoot of the drain-source voltage is plotted against the normalized temperature of the switched transistor. The actual temperature is normalized to the temperature resulting from the initial gate drive signal with 5 ns rise and fall time. The system is not only considered in the steady state from the electrical point of view but also from the thermal point of view. The system efficiency is proportional to the transistor temperature. Applying the resistor approach, the maximum overshoot of u_{ds} is decreased from 29.3 V to 26.0 V while the normalized temperature is increased by about 5.05 %. In contrast, $u_{\mathrm{ds,max}}$ is decreased from 29.3 V to 25.9 V applying the proposed AGD approach as described in section III.C while the normalized temperature is only increased by 0.4 %. It follows that the trade-off between EMC and efficiency can be significantly improved by applying the proposed AGD approach in comparison to reduce the maximum overshoot by increasing only the switching times.

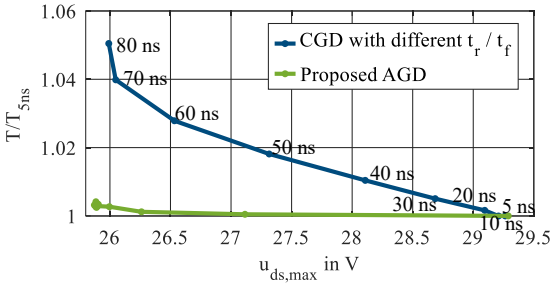

Fig. 12: Maximum overshoot of the drain-source voltage against the normalized measured surface temperature of the switched transistor for a CGD with different rise and fall times and the proposed AGD

E. Analysis of the Optimization Parameters

In section III.B the entire spectrum of the gate drive signal is optimized. To reduce the computation effort and the amount of time, in section III.C only the real and imaginary part of one harmonic is optimized. The optimization of a different number of harmonics is discussed in [15]. Similar observations should be made here on the efficiency, the maximum overshoot of u_{ds}, the needed number of iterations until termination of the optimization process and the computational effort, measured by the number of necessary measurements in each iteration step if the gradient has to be determined, as the performance criteria. As in the simulation shown in [15] the number of optimized harmonics is here increased to three and the same approach as described in III.C is performed with the difference, that the harmonics at 17 MHz, 23 MHz and 51 MHz are optimized. The choice of the optimized harmonics is based on the results of [15] and the possibility to generate the optimized gate drive signal found by the optimization of the entire spectrum in III.B. The performance criteria for the two configurations are shown in Fig. 13. The computational effort increases by the optimization of 3 harmonics to 13 measurements in each iteration step from 5 measurements if optimizing one harmonic. This is caused by

the determination of the gradient. In contrast, optimizing one harmonic, the AGD method is terminated due to the maximum number of the allowed 20 iterations and the value of the objective function remain still at about $3 \cdot 10^{-4}$ while the optimization of three harmonics is terminated after 12 iterations with an objective function of $7 \cdot 10^{-8}$. The difference regarding the maximum overshoot of u_{ds} is very small with $\Delta u_{\mathrm{ds,max}} = 0.08\,\mathrm{V}$. Considering the temperature, in both cases, the measured temperature of the transistor is 79.1 °C at the beginning of the optimization. The temperature at the end of the optimization of one harmonic is 79.4 °C and by optimizing three harmonics only 79.0 °C. The small reduction of the power losses can also be observed in simulation and can be justified with a more efficient switching slope in contrast to the linear edge of the initial conventional gate drive signal. All in all, the optimization of more harmonics of the gate drive signal leads only to a small improvement of the trade-off between EMC and efficiency and a better convergence behavior at the cost of a higher computation effort in each iteration.

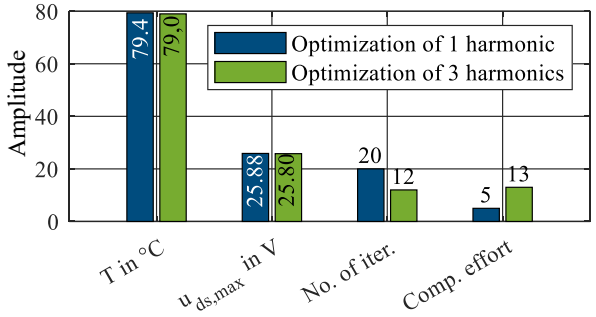

Fig. 13: Comparison of the resulting temperature, maximum overshoot of u_{ds}, the number of needed iterations until termination and the computational effort after the application of the proposed AGD approach in the measurement setup while optimizing one or three harmonics of U_g respectively

IV. Conclusion

Electromagnetic interferences can be caused by power electronic converters. Controlling the gate of a switched transistor by active gate driving methods is a possible countermeasure to reduce the disturbances. In this paper the overshoots after the switching events which result in a narrowband peak in the frequency spectrum have been reduced. The Levenberg-Marquardt method is used in the frequency domain to determine the necessary gate drive signal to reach this target. This approach is applied to the switched low-side transistor of a DC/DC boost converter in simulation and in a laboratory setup. The harmonic with the highest amplitude in the disturbing peak is reduced by 15 dB in simulation and measurement. In measurements the proposed approach is compared to inserting an additional gate resistor for reducing the disturbances. Here, the rise and fall time of the gate drive signal are increased. The trade-off between the EMC and the efficiency is much improved by applying the proposed AGD method. A further improvement of this trade-off can be reached by optimizing more harmonics of the gate drive signal at the cost of an increased computation effort. A multi-criterial optimization, e.g., considering the efficiency in the objective function, is a possible option for the expansion of this AGD method.

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