Broadband Active Common Mode EMI Suppression of Motor Inverters with Adaptive FIR Filters Using Delay-Compensated Digital Gate Control Signals

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Abstract—Due to advances in power transistor technologies, such as wide-bandgap semiconductors, higher switching frequencies and steeper switching slopes are used in power electronic systems to achieve higher efficiency and power density. However, this leads to increased electromagnetic interference (EMI). Conventional passive filter topologies can use a considerable amount of space and contain heavy components, reducing overall power density. To minimize volume and weight of passive filters, active EMI filters can be used. In this work, a novel EMI cancellation method is presented, which uses the gate control signals of a power electronic system to generate a cancellation signal, which is then superposed with the disturbance signal. The control signals are slightly delayed to compensate for the time required to synthesize and inject the cancellation signal. The cancellation system contains a digital adaptive filter to calculate the cancellation signal and to achieve high noise suppression. First, the used method is described in general. After that, the applicability to power electronic systems is discussed. For demonstration, the cancellation system is applied to a motor inverter to reduce the conducted common mode EMI (CM EMI) caused at the input side of the inverter. The results are shown and discussed for different operation modes.

Keywords—Active EMI filter, common-mode EMI, motor inverter

I. INTRODUCTION

Due to increasing conducted EMI caused in power electronic systems through high switching frequency and steep switching slopes, active EMI filters have been investigated in recent years. In general, most active EMI filters have in common that noise suppression is achieved by generating a cancellation or anti-noise signal that is superposed with the noise signal. For this, active EMI filters are composed of noise-sensing, noise-processing and anti-noise-injecting components [1]. While there are different variations of noise-sensing and noise-injecting circuits, such as capacitive or inductive circuits, another differentiation of active EMI filters is found in the principle of the noise-processing circuit. Here, various approaches have been investigated. Analog noise-processing circuits, consisting of passive components and an analog active circuit, have been used for noise suppression in dc-dc-converters [2], [3], ac-dc-converters [4] and motor inverters [5], [6], [7]. In [7] in particular, the line voltages of a motor inverter are measured and then converted to a fitting cancellation common-mode current by an amplifier and a passive circuit, matching the previously measured motor CM impedance. The achieved noise reduction is 33 dB at 150 kHz, 15 dB at 1 MHz and 0 dB above 2.5 MHz. Besides analog circuits, digital noise-processing concepts may be implemented [8], [9]. Here, a digital system, such as an FPGA or a DSP, is used in conjunction with analog-digital converters (ADC) and digital-analog converters (DAC) to sample, process and inject the noise and the anti-noise signals. Other approaches use synthesized cancellation signals rather than the sensed noise signals. In [10], CM disturbance pulses of a dc-dc converter

are suppressed using a synchronized 2-level compensation pulse. This way, a broadband suppression of 25 dB and up to 55 dB is achieved in a frequency range of 150 kHz to 1.8 MHz. [11] follows a similar approach using a synchronized CM compensation pulse for a dc-dc converter. In contrary to [10], the anti-noise signal is synthesized with a DAC instead, allowing for adjustment of shape, amplitude and width, resulting in a suppression of 10 dB at 150 kHz and up to 30 dB at 10 MHz. In [12], [13], [14], individual noise harmonics are cancelled by using adaptive notch filters, which are based on the continuous adaptation of the phase and amplitude of sinusoidal cancellation signals. For individual frequencies, reductions of up to 56 dB for the differential mode EMI of a dc-dc converter have been achieved [12]. Another approach, investigated in [15], [16], [17], is the injection of synthesized and synchronized signals. This method is based on the measurement of one or more periods of the noise signal, which is processed into a periodic cancellation signal. While limited to quasi-periodic disturbances, broadband noise suppression from 47 dB up to 65 dB in a frequency range of 150 kHz to 30 MHz have been achieved for the CM EMI of a motor inverter using this method [15].

When considering broadband noise reduction, each method has drawbacks that limit the achievable noise suppression or applicability. For analog and digital noise-processing circuits, the limiting factors are propagation delays inside of the active filter, causing a phase misalignment of the disturbance and cancellation signal [18]. Adaptive notch filters evade this issue, but the suppression is limited to certain harmonics [12], a narrow frequency range [13] or strictly periodic disturbance [19]. The injection of synthesized and synchronized signals achieves high suppression over a wide frequency range but is limited to quasi-periodic EMI and requires complex laboratory devices [15]. Therefore, a novel cancellation method, based on an adaptive **f**inite **i**mpulse **r**esponse (FIR) filter, is developed for broadband feedforward noise suppression of power electronic systems. Due to the feedforward concept, the active filter is not limited to periodic EMI. To mitigate limitations related to propagation delays of the filter, the digital control signals of the power electronic system are used as an input signal and are slightly delayed before entering the power electronic circuit. This allows for a compensation of propagation delays of the filter while maintaining the feedforward characteristic. Therefore, in the following this type of filter is called **d**elayed **d**igital **c**ontrol **d**igital **a**ctive EMI **f**ilter (DDC-DAEF). The active filter can be implemented using an FPGA system with ADCs and DACs and additional amplifier circuits.

The organization of the paper is as follows. First, a theoretical description of the cancellation algorithm is given. After that, the transfer of the algorithm to power electronic systems is analyzed. Here, requirements on the targeted system are identified. After that, a motor inverter demonstrator setup is introduced and analyzed regarding the

applicability on the cancellation of the CM EMI. Then, the implementation of the cancellation method using an FPGA system is described. Finally, the demonstrator results are shown and discussed, yielding a broadband suppression of ≈25 dB from 200 kHz up to 6 MHz. At 30 MHz still a significant reduction of ≈6 dB can be achieved.

II. Description of the cancellation algorithm

In this section, the proposed cancellation method is described. First, the underlying Filtered-X **l**east **m**ean **s**quares (LMS) algorithm is introduced. After that, the general description of the algorithm is transferred to power electronic systems, assigning the components of the electrical domain to the general model of the cancellation method. Finally, requirements and assumptions are derived that must be fulfilled by the power electronic system to successfully implement the cancellation algorithm.

A. General adaptive filter topology

Adaptive filters have been described by Kuo and Morgan in [20]. A general block diagram for an adaptive feedforward filter is depicted in Fig. 1. This figure shows an input signal $x(n)$, which traverses the primary path $P(z)$ and results in the noise signal $d(n)$. In parallel to the primary path, the adaptive filter with the transfer function $W(z)$ is located. The same input signal $x(n)$, that causes the noise signal, also traverses the filter $W(z)$ to form the cancellation signal $y(n)$. The cancellation signal and the noise signal are superposed to the residual noise signal $e(n)$. Ideally, the adaptive filter exactly resembles the primary path so that the residual noise signal $e(n)$ is cancelled out to $e(n) = 0$:

$$P(z) = W(z)$$
$$p(n) = w(n) \tag{1}$$

$$e(n) = d(n) - y(n)$$
$$= x(n) * p(n) - x(n) * w(n) = 0 \tag{2}$$

Where $p(n)$ and $w(n)$ are the respective impulse responses of the primary path and the filter and $*$ denotes the convolution operator.
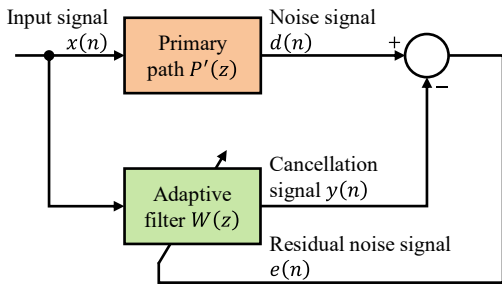

Fig. 1. General block diagram of active noise cancellation using an adaptive filter [20].

B. Filtered-X LMS algorithm

As described in the previous section, the optimal filter transfer function for the adaptive filter is $W(z) = P(z)$. However, in practical applications, this optimal transfer function might not be available due to e.g., lacking information on the primary path transfer function. In addition, the filter might not be able to fully represent a primary path with a high complexity. In these situations, an adaptive filter can be used, which consists of a filter with variable coefficients and an adaptive algorithm to iteratively calculate

these coefficients [20]. One popular adaptive algorithm is the LMS algorithm, which minimizes the mean value of the squared error signal $e^2(n)$ by parameterizing a finite impulse response filter. The output signal of an FIR filter with order M can be written as follows [20]:

$$y(n) = w_0 x(n) + w_1 x(n-1) + \cdots + w_M x(n-M)$$
$$= \boldsymbol{w} \cdot \boldsymbol{x}(n) \tag{3}$$

Where $\cdot$ denotes the dot product of the two vectors, $\boldsymbol{w} = (w_0 \quad \cdots \quad w_M)$ is the filter coefficient vector and $\boldsymbol{x}(n) = (x(n) \quad \ldots \quad x(n-M))$ is the input signal vector, consisting of the last $M+1$ samples of the input signal. Using the input signal vector and the error signal, the LMS algorithm iteratively adapts the filter coefficient vector according to the following update rule [20]:

$$\boldsymbol{w}(n+1) = \boldsymbol{w}(n) + \mu \boldsymbol{x}(n)e(n) \tag{4}$$

Where μ is the step size of the LMS algorithm. After convergence, the filter weight vector is optimal in terms of minimizing the mean squared error signal [20]. The LMS algorithm is widely used in acoustic applications [21], [22] because of the small number of operations needed when compared to other adaptive algorithms (e.g., recursive least squares algorithm) [20]. This reduces the computing power needed for real-time implementation, even though the convergence speed is slower compared to said alternatives [20].

The topology depicted in Fig. 1 assumes that all signals exist in the signal processing domain and are directly accessible. However, in practical applications, the cancellation takes place in, e.g., the acoustical or electrical domain, and all relevant signals have to be converted between the signal processing domain and the respective physical domain [20]. Therefore, the system description of Fig. 1 must be extended by an injection path and a sensing path, which is shown in Fig. 2. The injection path is located at the output of the adaptive filter and converts the digital cancellation signal into a physical cancellation signal that interferes with the noise signal in the physical domain. The sensing path is located in the feedback loop of the error signal and converts the physical residual noise signal into a digital signal that can be processed by the algorithm.
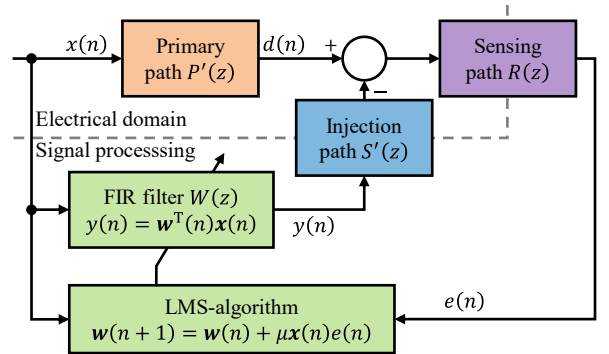

Fig. 2. Extended block diagram of active noise control using the LMS algorithm and injecting / sensing circuits for accessing the physical signals [20].

To simplify this new topology, the injection path and the sensing path are collapsed into a secondary path $S(z)$ that is located at the output of the adaptive filter. As the secondary path affects the cancellation signal before the superposition

with the noise signal, it must be considered in the LMS algorithm (4) to ensure stability [23], leading to the introduction of the filtered-X LMS algorithm. In this algorithm, the input signal vector $\boldsymbol{x}(n)$ is filtered by the secondary path $S(z)$:

$$\boldsymbol{x}'(n) = \boldsymbol{x}(n) * s(n)$$
$$X'(z) = X(z)S(z) \tag{5}$$

Where $s(n)$ is the impulse response of the secondary path. The resulting filtered-X LMS update rule is as follows:

$$\boldsymbol{w}(n+1) = \boldsymbol{w}(n) + \mu\boldsymbol{x}'(n)e(n) \tag{6}$$

In practical implementations, the exact secondary path transfer function $S(z)$ is not available, therefore a sufficiently accurate secondary path model $\hat{S}(z)$ is used. In [24], it has been found that the phase shift of the model has to match the phase shift of the exact transfer function by $< \pm 90°$. The resulting diagram including the secondary path and the filtered-X LMS algorithm is shown in Fig. 3.
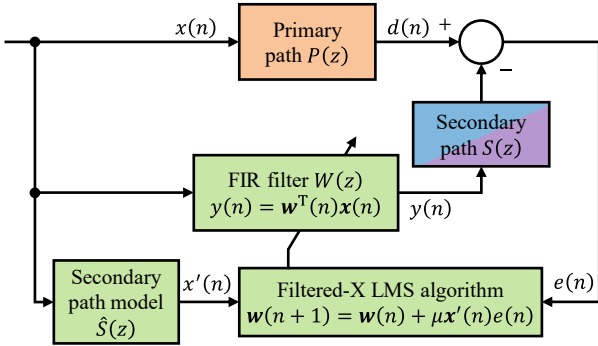

Fig. 3. Extended block diagram of active noise control with the secondary path $S(z)$ and the model $\hat{S}(z)$ [20].

C. Theoretical application in power electronic systems and fulfilment of the causality constraint

To identify the applicability of the derived filtered-X LMS algorithm in digital active EMI filters for power electronic systems, the theoretical description must be transferred to the typical topology of power electronic systems. In this work, only line-conducted interferences at the input or supply of the power electronic system shall be considered.

In general, when analyzing electromagnetic disturbances of power electronic systems, the noise signal may be modeled through a disturbance current or voltage, which can be interpreted as the input signal $x(n)$. As the sink of the disturbance shall be an artificial network at the supply lines of the system, the primary path $P(z)$ contains all elements up to said artificial network, such as passive filters, power lines, parasitic couplings etc. Therefore, the noise signal $d(n)$ is the result of the disturbance current or voltage traversing the primary path up to the artificial network. To introduce the anti-noise signal into the system, an injection circuit is needed. Such injection paths have been thoroughly described in [1] and might contain a DAC with capacitive or inductive couplers to inject the anti-noise into the supply lines. As a sensing circuit for measuring the input signal $x(n)$ and the residual noise signal $e(n)$, capacitive or inductive sensing circuits [1] may be used in conjunction with an ADC. Finally, a digital signal processor (DSP) is needed to process the input signal and residual noise signal into the anti-noise signal according to the Filtered-X LMS algorithm.

In the previously described concept, the disturbance current or voltage traverses the primary path, while, in parallel, it has to be measured, processed into the anti-noise signal and injected. However, for a successful cancellation, the noise and anti-noise signal need to be correctly aligned in time, which is known as the causality constraint [20]. The causality constraint requires the delay δ_P of the primary path to be equal or greater than the total delay of the adaptive filter δ_W and the secondary path δ_S:

$$\delta_\text{P} \geq \delta_\text{W} + \delta_\text{S} \tag{7}$$

Otherwise, the noise would change faster than the anti-noise can be adjusted accordingly, reducing the effectiveness of the cancellation, especially for high frequencies [12]. However, fulfilling the causality constraint poses a challenge for electrical systems, as the noise traverses the primary path at electrical propagation speeds. With the additional latency of, e.g., the DSP, ADC and DAC, it is highly unlikely that the primary path delay exceeds the secondary path delay. Contrary to that, in acoustical systems the noise traverses the primary path at the speed of sound, allowing for a much larger delay in the processing of the digital anti-noise signal.

There are multiple approaches to fulfill the causality constraint. One countermeasure is to assume the noise signal as a periodic signal and to store one period of the input signal in the DSP. The repeating sequence could then be re-aligned so that the delay of the DSP and secondary path is compensated. However, this is feasible for steady-state systems only, as the noise might vary for different operating points of the system. In addition, the required storage capacity can be very high, depending on the fundamental frequency of the noise and the required sample rate. Another approach is to use narrowband sinusoidal input signals to suppress individual frequencies, which has been pursued in [12], [13], [14]. In this work, however, a new approach is developed where the switching signals of the power electronic system are used to process the anti-noise signal. This approach is feasible as the EMI of power electronic systems are usually a causal result of the switching events inside the system, and the digital control signals can be easily delayed before reaching the power transistors. This way, the total delay of the primary path, which now starts at the origin of the gate control signals, can be increased to match the total delay of the active filter and the secondary path. A block diagram of the proposed method is shown in Fig. 4.
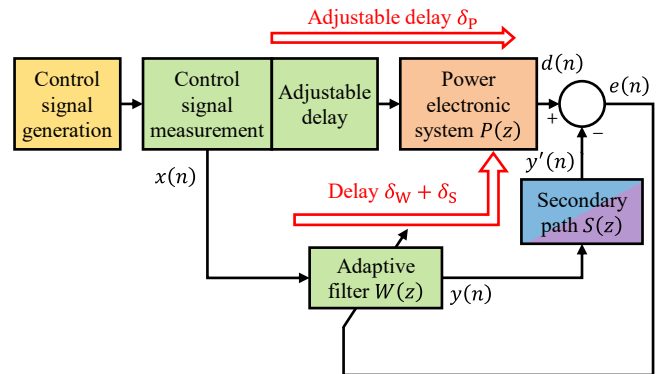

Fig. 4. Block diagram of proposed concept to fulfill the causality constraint.

D. Requirements on the power electronic system

Based on the previous theoretical description of the cancellation method, the requirements on the power electronic system can be derived.

1) The noise signal must be a superposition of the step responses of the switching slopes of the control signals:

As discussed in section II.C, it is required to use the control signals of the transistors as the input signal $x(n)$ of the filter to fulfill the causality constraint. In turn, this requires a direct connection between the control signals and the noise signal that can be matched and recreated by the FIR filter. Concerning binary gate control signals, each rising or falling slope can be represented as a step function. The resulting noise signal must be only the superposition of the primary path step responses to the binary gate control signals. At the summation point, the step responses of both the primary path and the adaptive FIR filter are added, resulting in noise reduction. Noise of other origin cannot be suppressed.

2) Step responses of the control signals must be sufficiently short:

As an adaptive FIR filter is used due to its stability and the ease of its digital implementation, the complexity of the output response is limited. Again, for binary gate control signals as input $x(n)$, the FIR filter step response reaches a constant output level after the length of its finite impulse response has passed. For the anti-noise to match the noise, the step response of the primary path has to reach a constant output level in equal or less time than the FIR filter. Therefore, short switching noise pulses are favorable for this method. As the disturbance mechanism, or primary path, varies for each power electronic system, the system of interest must be analyzed individually.

III. DEMONSTRATOR SETUP AND ACTIVE CANCELLATION IMPLEMENTATION

In this section, results using a demonstrator setup are shown. First, the power electronic demonstrator, consisting of a 48 V motor inverter system, is described. Following that, the applicability of the proposed method in this system is analyzed. After that, the active cancellation system is implemented to reduce the common mode EMI at the DC terminals of the motor inverter. In the last chapter, the test results are shown.

A. Motor inverter system

The demonstrator setup is a 48 V motor inverter system which has been already presented in [15] to demonstrate the results of the active cancellation using synthesized and synchronized signals. The setup consists of a 48 V voltage source, two artificial networks for EMI measurements, a 48 V GaN motor inverter and a motor load emulation consisting of inductors and resistors, which is later substituted for a synchronous motor in section IV.E. At the DC side of the system, the DC− line is isolated from the ground, so that CM currents can occur in both DC lines and the electrical ground of the system. The measurement ports of the artificial networks are connected using a common/differential mode switch (CM/DM switch) from Schwarzbeck, CMDM 8700, which contains a high frequency transformer with multiple windings. At the output of the common/differential mode switch, the DM EMI of the DC lines are subtracted, while the CM EMI are preserved. Finally, an EMI test receiver by R&S, ESRP, is connected to the switch, measuring the CM EMI at the inverter DC input. A block diagram of the overall setup is depicted in Fig. 5.
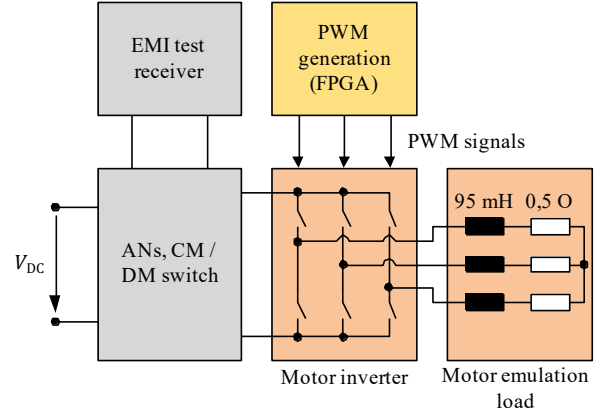

Fig. 5. Simplified block diagram of the demonstrator inverter system [15].

The inverter is controlled by sinus-modulated PWM signals, determining the switching states of the half-bridges inside of the inverter. The PWM signals are calculated by a separate FPGA system. The fundamental switching frequency of the PWM signals is 100 kHz, with a varying modulation frequency depending on the requested motor speed.

B. Analysis of the applicability of the proposed cancellation method

As discussed in section II.D, the applicability of the proposed cancellation method requires the noise signal to consist of multiple step responses, as the used adaptive FIR filter may only reproduce step responses as output signals. Therefore, the underlying mechanism of CM EMI in inverter systems has to be analyzed.

In, e.g., [7], [25], [26], it is shown that CM EMI in inverter systems is primarily caused by parasitic capacitive coupling between the motor lines and the electrical ground, e.g., the housing of the motor or shielding of the motor cables. This capacitive coupling forms a low impedance path for high frequency currents, generated through the switching output voltages of the motor inverter. The return path of the CM current usually consists of additional capacitive coupling between the DC lines and the electrical ground, consequently causing CM interferences at the DC side of the system. In this setup, the return path through the DC lines is defined through the discrete components inside of the artificial networks, the CM switch, and the EMI test receiver. The resulting voltage drop caused through the CM current at the EMI receiver is eventually measured as the CM EMI at the DC side.

To analyze this mechanism, a model of the CM EMI must be introduced. Therefore, an equivalent one-phase model according to [7] is used, which is depicted in Fig. 6. This model consists of a CM voltage source V_{CM}, the capacitive coupling $C_{3ph,GND}$ of the three load phases to ground, the equivalent impedance $Z_{load,GND}$ of the load to ground, and the equivalent impedance $Z_{AN,GND}$ of the artificial networks to ground. To introduce the EMI test receiver and therefore the measured CM EMI $V_{CM,EMI}$ as part of the model, the impedance Z_{Rec} of the EMI test receiver is added.
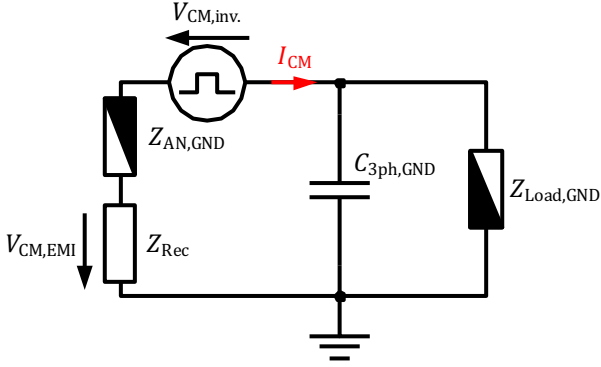
Fig. 6. Equivalent single-phase model with the motor inverter as a CM voltage source $V_{\text{CM,inv.}}$ causing the CM current I_{CM} [7].

The occurring CM voltage $V_{\text{CM,inv.}}$ consists of the sum of the line voltages V_{a0}, V_{b0} and V_{c0} to ground, which is described through the formula (8) [7]:

$$V_{\text{CM,inv.}} = \frac{V_{\text{a0}} + V_{\text{b0}} + V_{\text{c0}}}{3} \qquad (8)$$

Each line voltage to ground is determined by the switching state x_{a}, x_{b} and x_{c} of each half bridge:

$$V_{\text{a0/b0/c0}} = \begin{cases} +\dfrac{V_{\text{DC}}}{2} & x_{\text{a/b/c}} = 1 \\[2mm] -\dfrac{V_{\text{DC}}}{2} & x_{\text{a/b/c}} = 0 \end{cases} \qquad (9)$$

The resulting CM voltage measured at the port of the EMI test receiver can be described with:

$$V_{\text{CM,EMI}} = \frac{V_{\text{a0}} + V_{\text{b0}} + V_{\text{c0}}}{3} \cdot \frac{Z_{\text{Rec}}}{Z_{\text{eq,CM}}} \qquad (10)$$

In equation (10), $Z_{\text{eq,CM}}$ denotes the total CM impedance of the system, defining the total CM current caused by the motor inverter.

The introduced model shows that a system definition with the half bride control signals $x_{\text{a/b/c}}$ as input signals and the CM disturbance $V_{\text{CM,EMI}}$ as the output signal can be derived. Therefore, the proposed active cancellation method is applicable to the system if a suitable input signal related to the inverter CM voltage is used.

C. Implementation of the active cancellation system

After analyzing the applicability of the proposed method, the active cancellation system is implemented in the motor inverter system.

a) FPGA system: For real-time implementation of the FxLMS-algorithm introduced in section II.B, the FPGA system STEMlab 125-14 by Red Pitaya is used. This FPGA board contains a Xilinx Zynq 7020 SoC, which is connected to two ADCs and two DACs. All four converters provide a vertical resolution of 14 bit and a sample rate of 125 MS/s. The overall system is capable of processing analog signals with a bandwidth greater than 50 MHz. The FPGA is clocked at the same frequency of 125 MHz, i.e., one step of the filter algorithm is computed in 8 ns, a new input sample is loaded and a new output sample is injected. The FPGA is configured using MATLAB and Simulink HDL coder. This way, the

algorithm can be defined though a block diagram, which is then synthesized into Verilog code to program the FPGA.

b) Delay of the control signals: As discussed in section II.C, the causality condition has to be met to successfully suppress noise using this method. To do so, the total signal delay of the noise or primary path has to be equal or greater than the total signal delay of the anti-noise, with both paths starting at the noise source as shown in (7). However, it can be assumed that this condition is not met in the motor inverter system, as the delay of the half bridge driver logic, drivers and transistors is very low. However, the control signals can be delayed before reaching the driver circuits, effectively adding a propagation delay to the primary path. This can be done by digital delay generator ICs, or, in this case, the FPGA system placed inbetween the control signal source and the motor inverter. This way, the anti-noise signal can be calculated based on the control signals while simultaneously delaying the control signals to compensate for the total latency of the anti-noise calculation and injection.

c) Input signal calculation: In parallel to the delay of the half bridge control signals, a viable input signal x for the algorithm has to be calculated, as seen in section III.B. To do so, a signal proportional to the inverter CM voltage is derived based on equation (11):

$$x = x_{\text{a}} + x_{\text{b}} + x_{\text{c}} - 1.5 \propto V_{\text{CM,inv.}} \qquad (11)$$

The resulting signal is shifted by -1.5 so that the DC component is 0. Compared to a direct calculation of $V_{\text{CM,inv.}}$, this proportional signal is unaffected by the inverter DC input voltage V_{DC}, while the scaling of the amplitude is managed by the weights of the algorithm. Therefore, this unscaled signal is advantageous and does not require measuring V_{DC}.

d) Noise sensing circuit: To sense and feed back the residual CM noise signal as the error signal $e(n)$, the measurement port of the CM/DM switch is used. To distribute the signal between the EMI receiver for measurements and the active filter, a power splitter is used. The power splitter is connected to one of the ADCs of the FPGA system, which is connected in parallel to a 50 Ω resistor for line termination.

e) Anti-noise injecting circuit: To inject the calculated anti-noise signal back into the system, an injecting circuit is needed. For this, capacitors are used providing high-frequency coupling to the DC-lines. The cancellation signal is generated with the DAC of the FPGA system and then amplified by a high power, high frequency operational amplifier board ADA4870ARR-EBZ. For a higher gain, both FPGA DACs are used with one amplifier each, so that the cancellation current is not split across both DC lines. However, both outputs generate exactly the same signal. In order not to short the cancellation signal by the inverter bulk capacitors, a CM choke of the type WE MnZn 74272722 by Würth Elektronik is added between the coupling capacitors and the input of the inverter. Even with the cancellation signal disabled, the CM choke filters the CM EMI measured at the DC lines, which has to be considered when the performance is evaluated in Section IV.A.

A diagram of the overall setup, including the FPGA system, the sensing, and the injecting circuit, is depicted in Fig. 7. A picture of the laboratory setup is shown in Fig. 8.
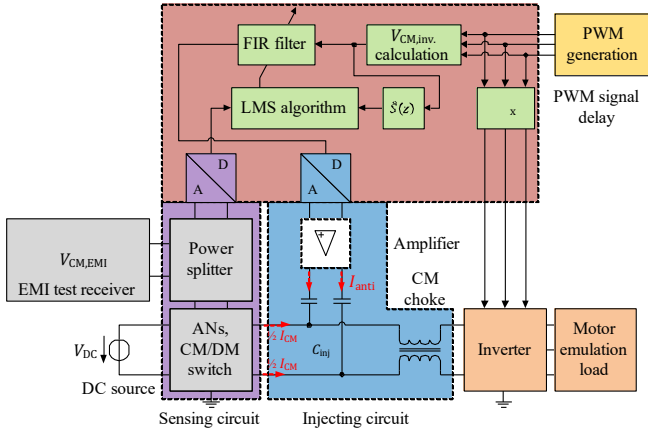
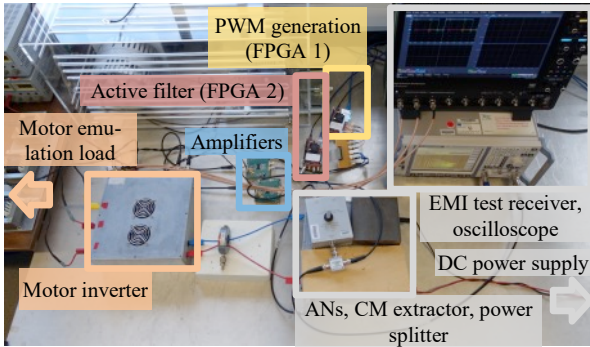Fig. 7. Block diagram of the overall test setup.

Fig. 8. Laboratory test setup.

IV. Measurement Results

In this section, the demonstrator measurement results are shown and discussed. Furthermore, some transient scenarios are analyzed to point out advantages and limitations of the proposed cancellation method.

A. CM EMI without and with disabled cancellation system

First, the CM EMI without the cancellation system is measured. The operation parameters of the system are set to a DC voltage of 24 V and a modulation frequency of 50 Hz. The total power dissipated through the motor emulation is ≈230 W. In Fig. 9 (bottom plot), the CM noise measured at the common/differential mode switch with an oscilloscope is shown in time domain. Additionally, the measured PWM control signals are shown in the upper plot, which are then used to calculate the CM inverter voltage in the center plot according to (8). In this graph, the correlation of the PWM signals and the disturbance signal, as discussed in section III.B, is apparent: Each negative step of the CM inverter voltage causes a short CM EMI pulse of +3 V, while the steep positive steps at ≈0 μs and ≈10 μs causes CM EMI pulses of −9 V. In turn, the CM inverter voltage directly relies on the PWM signals: As all half-bridges are switched on at ≈10 μs, the CM inverter voltage rises, while the turn-off of each individual half-bridge causes the CM inverter voltage to drop by ⅓.

In Fig. 10, the EMI test receiver CM noise voltage measurements without and with cancellation system in a disabled state are shown. It must be noted that the CM choke and coupling capacitors are only included in the scenario with the cancellation system in a disabled state. The measurements are conducted using a resolution bandwidth of 9 kHz and a measurement time of 20 ms to record one full period of noise.

The disturbance consists of switching harmonics at multiples of 100 kHz, which corresponds to the PWM modulation frequency of the inverter. Comparing the spectra without and with cancellation system in a disabled state, a resonance at 500 kHz is introduced through the passive components of the cancelation system. This is assumed to be caused by the additional coupling capacitors and the CM choke. At higher frequencies, the CM choke and decoupling capacitors reduce the overall measured CM noise, even with the cancellation system disabled.
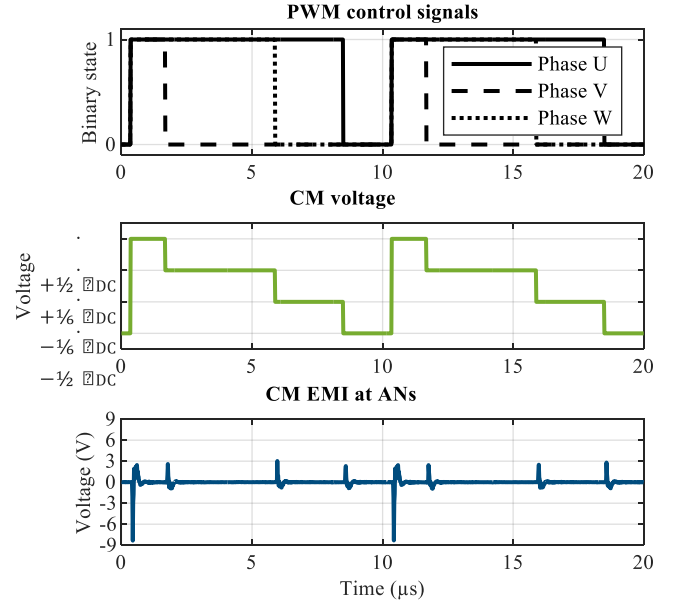

Fig. 9. Measured inverter control signals, calculated CM inverter voltage $V_{CM,inv.}$ and measured CM noise voltage $V_{CM,EMI}$ at the artificial network.
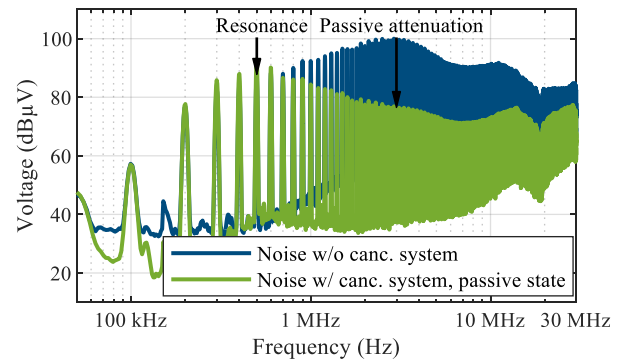

Fig. 10. Noise spectra without cancellation system and with cancellation system in deactivated/passive state (reduction through passive components of the system).

B. Secondary path identification and modeling

To ensure stable operation of the Filtered-X LMS algorithm, the secondary path $S(z)$ must be identified to find an adequate model $\hat{S}(z)$. To do so, the FPGA system injects a series of sine waves with different frequencies into the system while the inverter is turned off. This identification signal then traverses the secondary path and is measured by the FPGA system at the sensing circuit. By comparing the amplitude and phase of each sine wave at the input and the output of the system, a discrete transfer function of the secondary path can be calculated. Next, this frequency-discrete transfer function can be converted to a digital model that filters the input signal in real time like shown in (5). Here, a second-order IIR filter

is used in conjunction with a digital delay to account for the dead-time of the system. The latency may be caused by, e.g., FPGA processing latency, DAC and ADC latency, propagation delay of the signals through the cabling system and so on. A total delay of 26 samples is identified, which equals $26 \cdot 8\,\text{ns} = 208\,\text{ns}$. The parameters of the IIR filter are approximated using the MATLAB function *invfreqz* [27] on a PC. In Fig. 11, the measured system response and the system response of the identified secondary path IIR filter model with the identified delay are depicted. The amplitude response shows a resonance at 500 kHz, which matches the resonance observed in the measured CM EMI (Fig. 10). The phase response is composed of a frequency dependent characteristic (e.g., through the components of the sensing and injection circuit) and a linear phase decrease due to the delay of 26 samples (appearing exponentially due to the logarithmic x-axis scale). The stability range of $\pm 90°$ phase response error, as required by the filter algorithm [24], is displayed as well and not violated by the model.
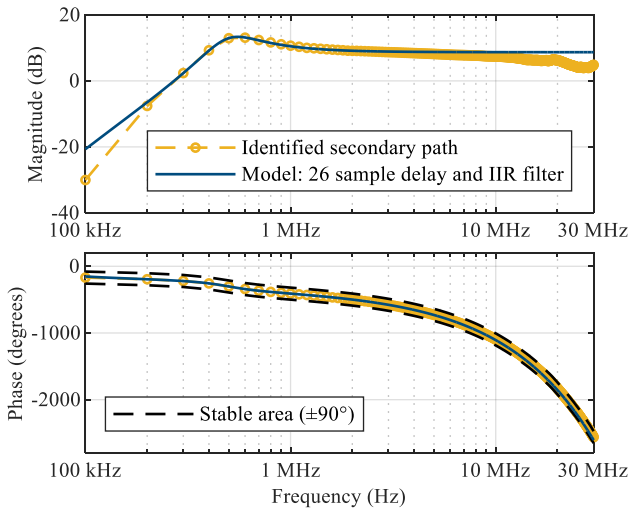

Fig. 11. Amplitude and phase response for the measured secondary path and the derived secondary path model consisting of a 26-sample delay and a second order IIR-filter.

C. CM EMI in power drive sytem with emulated motor

In the following, the noise compensation system is analyzed. First, the need of delaying the control signals in order to compensate for the processing delay of the FPGA, DAC, etc., is discussed. In Fig. 12 noise and residual noise without delaying the control signals are depicted. The residual noise almost exactly resembles the noise for $\approx 40\,\text{ns}$ after the pulse rises. This is because the cancellation system is unable to react to the disturbance pulse caused by the switching of the control signal in time. In Fig. 13, the same signals are depicted for an additional delay of 56 ns of the control signals. With the additional delay, the anti-noise signal can be processed in time to fully compensate the pulse of the noise signal. This delay must not be confused with the delay of 208 ns identified for the secondary path in section IV.B, as this delay of 56 ns only needs to account for the difference of latency in the primary path and the secondary path. The spectrum of the residual EMI is shown in Fig. 14, with the original noise without the cancellation system, and the reduced noise with the deactivated cancellation system. The noise is reduced across the depicted frequency range by $\approx 24\,\text{dB}$ up to 5 MHz, and $\approx 6\,\text{dB}$ at 30 MHz. At 100 kHz, the noise is reduced by $\approx 6.5\,\text{dB}$. As normative EMI emission tests only consider

frequencies above 150 kHz, this performance difference can be negligible for practical applications.
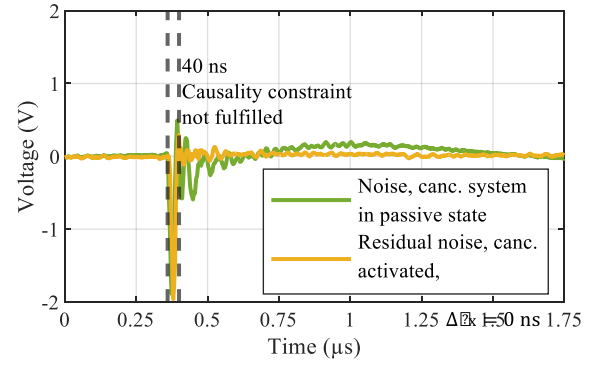

Fig. 12. Noise and residual noise after activating the cancellation system without additional delay of the control signals.
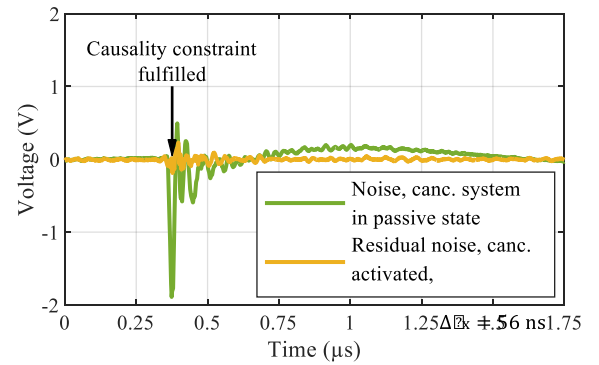

Fig. 13. Noise and residual noise after activating the cancellation system with an additional delay of the control signals by 56 ns.
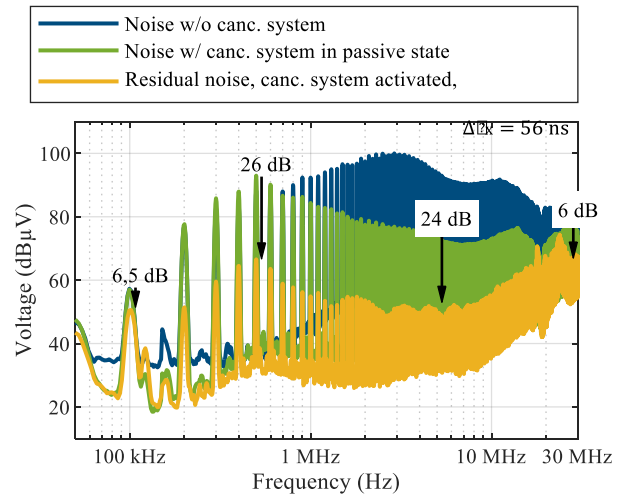

Fig. 14. Spectra of noise, noise with included but deactivated cancellation system and residual noise with activated cancellation system.

D. CM EMI cancellation for varying modulation frequency

In the previous section, the results have been discussed for a static modulation frequency of 50 Hz. However, in many use cases, e.g., for traction motors, the modulation frequency is changing over time. For a further investigation of the achievable noise suppression during load changes, measurements are conducted for a varying modulation frequency. To do so, the modulation frequency of the control signal generator is increased from 50 Hz to 100 Hz in steps of

2 Hz every 2 seconds, leading to a total of 48 seconds to ramp up to 100 Hz. The CM EMI is measured at each frequency step using the trigger input and the spectrogram mode of the R&S EMI test receiver. As the change of modulation frequency can only be seen in the side-band harmonics of the disturbance, the resolution bandwidth of the receiver is set to 10 Hz, while the frequency range is reduced to 198 kHz to 202 kHz to display the side-band harmonics adjacent to the switching harmonic at 200 kHz. To establish a baseline, the EMI with the cancellation system disabled is shown in Fig. 15. At 0 s, for which the spectrum is shown at the bottom, the side-band harmonics with a distance of 150 Hz around the switching harmonic at 200 kHz can be seen. The spacing of 150 Hz is caused through the symmetry of the three-phase system and the 120° phase shift of the control signals. Starting at 10 s in the spectrogram, the modulation frequency is increased. Therefore, the side-band harmonics are continuously spread with a wider distance. At 58 s, the maximum modulation frequency of 100 Hz is reached, for which the spectrum is shown at the top of the figure. Here, the spacing of the side-band harmonics is at 300 Hz.
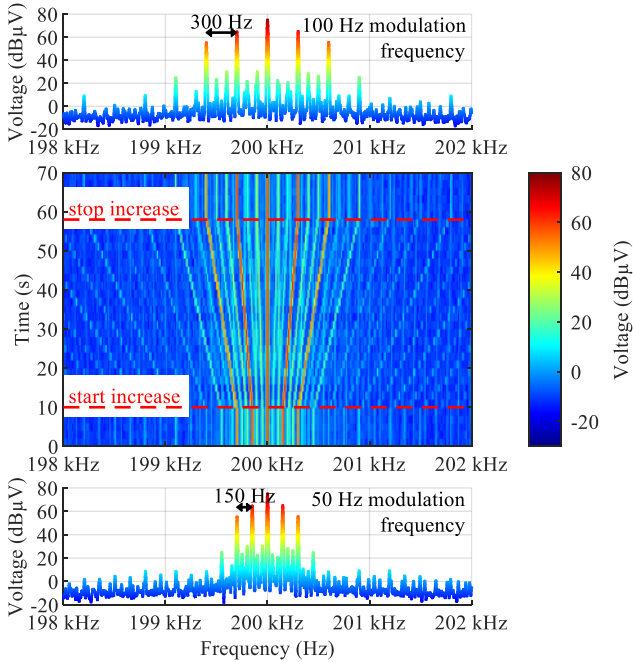

Fig. 15. Noise spectrogram with disabled cancellation system during frequency ramp from 50 Hz to 100 Hz.

For Fig. 16, the same procedure is conducted with the cancellation system enabled. As the cancellation system is enabled, the amplitude of each harmonic is reduced, which is represented through the color intensity of the spectrogram. Over the time of the frequency variation, the suppression is retained, as the amplitudes do not change. At 100 Hz modulation frequency, as shown at the top of the figure, each side-band harmonic is reduced by 25 dB up to 35 dB.
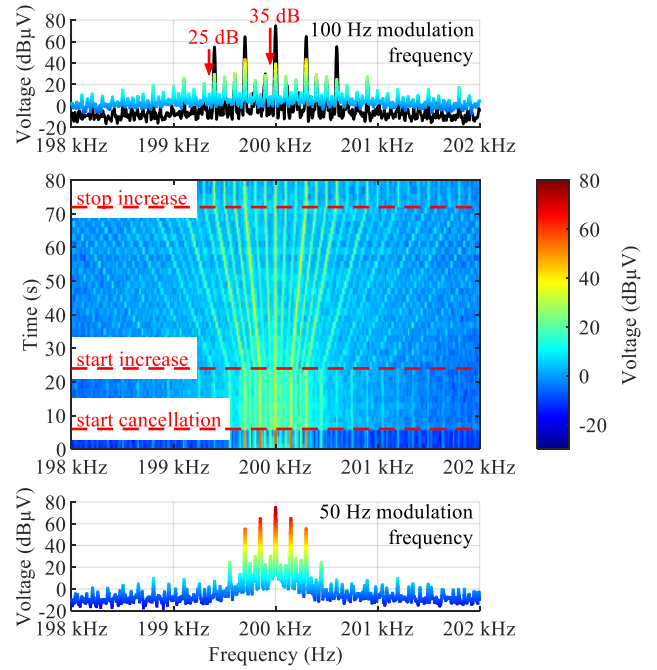
Fig. 16. Noise spectrogram with enabled cancellation system during frequency ramp from 50 Hz to 100 Hz.

It is expected that faster load changes can be compensated as well, as the adaptive FIR filter compensates each disturbance pulse based on each step in the input signal, $V_{\text{CM,inv.}}$. The motor frequency modulated through these pulses does not directly impact the shape of the noise pulses. Therefore, the proposed method is robust to changes in the input signal, given that the fundamental relationship between the switching events of the power transistors and the resulting disturbance pulses stay the same, which can be assumed in most cases.

Therefore, the power dissipated at the load is expected to have no influence on the noise suppression as well: Although the PWM modulated signals and time alignment of the pulses change, the voltage level of the inverter and consequently the individual disturbance pulses are unaffected, resulting in unchanged conditions for the noise suppression.

E. CM EMI in power drive system with PMSM

Up to this point, all measurements have been conducted using a motor load emulation with resistors and inductors. As real electric machines can lead to additional frequency components that can cause active compensation techniques to fail, in this section, the passive load is replaced by a 48 V **p**ermanent **m**agnet **s**ynchronous **m**otor (PMSM) with a variable mechanic load. The PMSM is controlled using a field-oriented control algorithm, running on a separate FPGA system. The injection and sensing circuits remain unchanged. However, as the motor introduces a different common mode impedance, which may affect the secondary path model, the secondary path model is updated using the same method as described in IV.B. Fig. 17 shows the transistor control signals and the resulting noise with the motor attached. The disturbance mechanism remains unchanged, as each switching signal results in a corresponding disturbance pulse. In comparison with the disturbance pulses with the motor emulation load in Fig. 9, the disturbance pulses with the PMSM are longer in time.
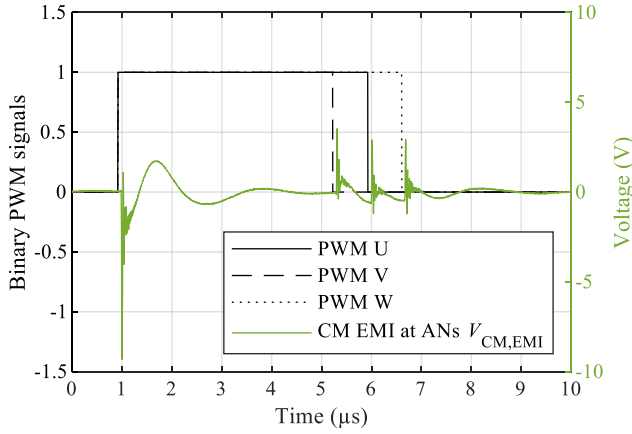
Fig. 17. Measured inverter control signals,and disturbance $V_{CM,EMI}$ at the artificial network for a 48V PMSM as load.

To investigate eventual dependencies of the dissipated mechanical power on the cancellation, the noise reduction performance is evaluated for two loads. In Fig. 18, the spectra of noise with deactivated cancellation system and the residual noise with activated cancellation system are shown for idle state with no mechanical load. Once more, the noise is reduced across the entire frequency range, with 23 dB at 600 kHz, 20 dB at 4 MHz, and still 6 dB at 10 MHz, yielding a result similar to the motor emulation circuit used for Fig. 14. The same measurement is repeated in Fig. 19 with a mechanical load. Once again, the cancellation yields nearly identical results, implying that the cancellation is not dependent on the total transfer power. This is plausible as the derived modeling of the CM disturbance in (8) and (10) only depends on the impedances of the system and the inverter voltage. In addition, this measurement shows the independency of the cancellation method on the PWM generation for the inverter: With the motor emulation load, pre-computed PWM signals were used, modulating an ideal sinusoidal waveform. For the PMSM, a field-oriented control algorithm was used, resulting in a more realistic application. As the cancellation is done for each individual switching impulse, the generation and sequence of these pulses do not affect the cancellation performance.
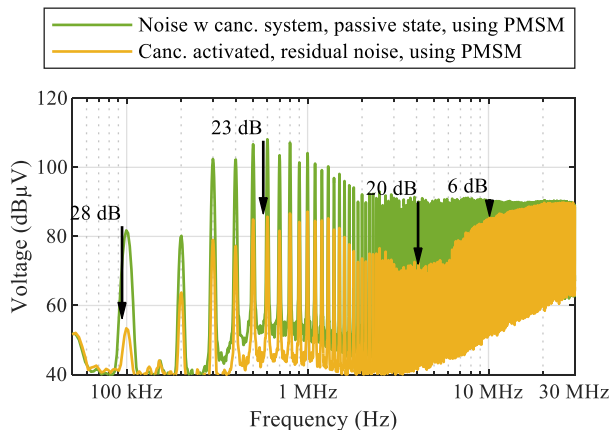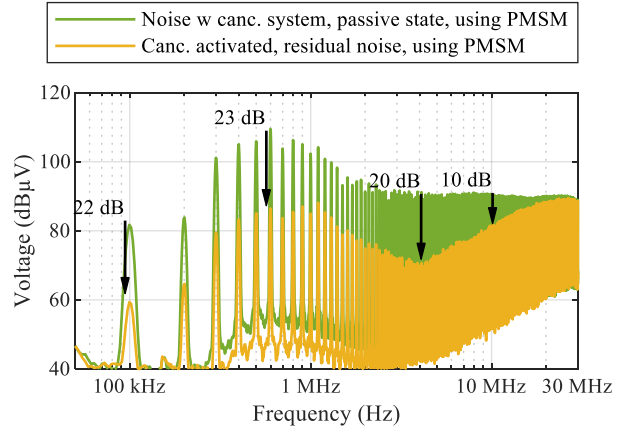

Fig. 18. Spectra of noise with deactivated and with activated cancellation system for a 48V PMSM with no mechanical load.

Spectra of noise with deactivated and with activated cancellation system for a 48V PMSM coupled to a mechanical load.

F. Power consumption of the CM EMI cancellation system

In order to assess the total impact of the EMI cancellation method on the system, the power consumption of the active circuitry has to be assessed. In this application, the FPGA system and the analog amplifiers need to be considered. An overview is given in TABLE I.

The measured power consumption for the FPGA system is about 5.5 W and is independent of the required cancellation power.

Furthermore, in the analyzed laboratory setup, the amplifier has a power consumption of about 2.4 W. However, the measured power of the cancellation signal is only about 70 mW. In comparison to the DC power of 260 W for the motor drive system, the power of the cancellation signal is very low, but due to the power consumption of the FPGA system and the amplifier, the EMI cancellation method requires 3.04 % of the motor drive system's power. To estimate the power consumption of the EMI cancellation method in a more realistic 100 kW powertrain system, the power of the cancellation signal is scaled by 100 kW / 260 W = 385. In this estimation it is already taken into account that the theoretical efficiency of 78.5 % [28] of a class B amplifier cannot be reached and an efficiency of 25 % is assumed. In this case, the EMI cancellation method would require only 0.11 % of the motor drive system's power.

TABLE I.   POWER REQUIRED FOR THE EMI CANCELLATION METHOD

	Measurement of 260 W low power system	Prognosis for 100 kW high power system
FPGA system	5.5 W	5.5 W
Cancellation signal	70 mW	27 W
Amplifier	2.4 W	108 W
Σ Power EMI cancellation method	7.9 W	113.5 W
Relation to transfer power in %	3.04	0.11

G. Delay of the PWM signals

Besides power consumption, another property that might influence the operation of the motor inverter system is the

introduction of the additional delay to the PWM signals in order to fulfill the causality constraint (section II.C). For the results as demonstrated in Fig. 18 and Fig. 19, a delay of 56 ns has to be introduced. Compared to the switching period of 10 µs, this delay is very short. Therefore, regarding the mechanical motor performance, no negative impacts are to be expected.

V. Conclusion

In this work, a novel cancellation method with an adaptive FIR filter, using the digital gate control signals as the input, has been presented to suppress the CM EMI of a motor drive system. With this method, the FIR filter weights are adapted using the filtered-X LMS algorithm to minimize the residual noise signal while considering effects by the injection and measuring path. Requirements on the power electronic system at issue have been derived. The causality constraint has been identified as a central condition that has to be fulfilled. To do so, the digital gate control signals are time shifted before reaching the power electronics to compensate the time needed for synthesizing and injecting the cancellation signal. The method has been applied to the CM EMI of both an emulated motor and a PMSM with similar results, using an FPGA system as a suitable signal processor for the cancellation method. The CM EMI has been actively suppressed by 20 dB up to 4 MHz and still 10 dB at 10 MHz. Additionally, it was shown that the CM EMI suppression is not influenced by speed changes. The cancellation signal's power of 70 mW is very small in comparison to the motor drive system's power of 260 W.

References

[1] B. Narayanasamy and F. Luo, "A Survey of Active EMI Filters for Conducted EMI Noise Reduction in Power Electronic Converters," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 6, pp. 2040–2049, Dec. 2019, doi: 10.1109/TEMC.2019.2953055.

[2] Y. Chu, S. Wang, and Q. Wang, "Modeling and Stability Analysis of Active/Hybrid Common-Mode EMI Filters for DC/DC Power Converters," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6254–6263, Sep. 2016, doi: 10.1109/TPEL.2015.2502218.

[3] D. Hamza, M. Sawan, and P. K. Jain, "Suppression of common-mode input electromagnetic interference noise in DC–DC converters using the active filtering method," *IET Power Electron.*, vol. 4, no. 7, p. 776, 2011, doi: 10.1049/iet-pel.2010.0200.

[4] R. Goswami, S. Wang, E. Solodovnik, and K. J. Karimi, "Differential Mode Active EMI Filter Design for a Boost Power Factor Correction AC/DC Converter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 1, pp. 576–590, Mar. 2019, doi: 10.1109/JESTPE.2018.2839734.

[5] S. Jeong, J. Park, and J. Kim, "A Customized Integrated Circuit for Active EMI Filter With High Reliability and Scalability," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12631–12645, Nov. 2021, doi: 10.1109/TPEL.2021.3083286.

[6] B. Narayanasamy, H. Peng, Z. Yuan, A. I. Emon, and F. Luo, "Modeling and Analysis of a Differential Mode Active EMI Filter With an Analog Twin Circuit," *IEEE Trans. Electromagn. Compat.*, vol. 62, no. 4, pp. 1591–1600, Aug. 2020, doi: 10.1109/TEMC.2020.3006427.

[7] Y. Zhang, Q. Li, and D. Jiang, "A Motor CM Impedance Based Transformerless Active EMI Filter for DC-Side Common-Mode EMI Suppression in Motor Drive System," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10238–10248, Oct. 2020, doi: 10.1109/TPEL.2020.2980881.

[8] D. Hamza and M. Qiu, "Digital Active EMI Control Technique for Switch Mode Power Converters," *IEEE Trans. Electromagn. Compat.*, vol. 55, no. 1, pp. 81–88, Feb. 2013, doi: 10.1109/TEMC.2012.2213590.

[9] J. Ji, W. Chen, and X. Yang, "Design and precise modeling of a novel Digital Active EMI Filter," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA: IEEE, Mar. 2016, pp. 3115–3120. doi: 10.1109/APEC.2016.7468309.

[10] D. Mueller, M. Beltle, and S. Tenbohlen, "EMI Suppression of a DC–DC Converter Using Predictive Pulsed Compensation," *IEEE Trans. Electromagn. Compat.*, vol. 63, no. 6, pp. 2134–2142, Dec. 2021, doi: 10.1109/TEMC.2021.3084896.

[11] Y. Zhang, Y. Liao, Q. Ren, H. Xu, Z. Huang, and C. Bi, "EMI Suppression of DC-DC Converters by Injecting Synthesized Pulse Signals," in *2023 6th Asia Conference on Energy and Electrical Engineering (ACEEE)*, Chengdu, China: IEEE, Jul. 2023, pp. 35–39. doi: 10.1109/ACEEE58657.2023.10239664.

[12] A. Bendicks, T. Doerlemann, S. Frei, N. Hees, and M. Wiegand, "Active EMI Reduction of Stationary Clocked Systems by Adapted Harmonics Cancellation," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 4, pp. 998–1006, Aug. 2019, doi: 10.1109/TEMC.2018.2854965.

[13] T. Doerlemann, A. Bendicks, and S. Frei, "FPGA-based Adaptive Notch Filters for the Active Cancellation of Varying Electromagnetic Emissions of Power Electronic Inverter Systems," in *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, Raleigh, NC, USA: IEEE, Jul. 2021, pp. 307–312. doi: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559297.

[14] J. Aigner, T. Doerlemann, A. Bendicks, and S. Frei, "Cancellation Path Identification for Effective Active EMI Filtering with Synthesized Signals in Inverters for Electric Powertrain Systems," in *2022 ESA Workshop on Aerospace EMC (Aerospace EMC)*, Virtual: IEEE, May 2022, pp. 01–06. doi: 10.23919/AerospaceEMC54301.2022.9828817.

[15] A. Bendicks, M. Gerten, and S. Frei, "Active Cancellation of Periodic CM EMI at the Input of a Motor Inverter by Injecting Synthesized and Synchronized Signals (S^3-AEF)," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11951–11961, Oct. 2022, doi: 10.1109/TPEL.2022.3172205.

[16] A. Bendicks and M. Gerten, "Active Cancellation of Periodic DM EMI at the Input of a GaN Motor Inverter by Injecting Synthesized and Synchronized Signals," in *2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Rome, Italy: IEEE, Sep. 2020, pp. 1–6. doi: 10.1109/EMCEUROPE48519.2020.9245768.

[17] A. Bendicks, M. Rubartsch, and S. Frei, "Simultaneous EMI Suppression of the Input and Output Terminals of a DC/DC Converter by Injecting Multiple Synthesized

Cancellation Signals," in *2019 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Barcelona, Spain: IEEE, Sep. 2019, pp. 842–847. doi: 10.1109/EMCEurope.2019.8871701.

[18] A. Bendicks, T. Doerlemann, S. Frei, N. Hees, and M. Wiegand, "Development of an Adaptive EMI Cancellation Strategy for Stationary Clocked Systems," in *2018 International Symposium on Electromagnetic Compatibility (EMC EUROPE)*, Amsterdam: IEEE, Aug. 2018, pp. 78–83. doi: 10.1109/EMCEurope.2018.8485063.

[19] A. Bendicks, T. Osterburg, S. Frei, M. Wiegand, and N. Hees, "Wide-Frequency EMI Suppression of Stationary Clocked Systems by Injecting Successively Adapted Cancellation Signals," in *2019 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Barcelona, Spain: IEEE, Sep. 2019, pp. 36–41. doi: 10.1109/EMCEurope.2019.8872019.

[20] S. M. Kuo and D. R. Morgan, "Active noise control: a tutorial review," *Proc. IEEE*, vol. 87, no. 6, pp. 943–975, Jun. 1999, doi: 10.1109/5.763310.

[21] S. M. Kuo, S. Mitra, and Woon-Seng Gan, "Active noise control system for headphone applications," *IEEE Trans. Control Syst. Technol.*, vol. 14, no. 2, pp. 331–335, Mar. 2006, doi: 10.1109/TCST.2005.863667.

[22] V. S. Nataraj, Athulya M. S., and S. P. Savithri, "Single channel speech enhancement using adaptive filtering and best correlating noise identification," in *2017 IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE)*, Windsor, ON: IEEE, Apr. 2017, pp. 1–4. doi: 10.1109/CCECE.2017.7946770.

[23] D. Morgan, "An analysis of multiple correlation cancellation loops with a filter in the auxiliary path," *IEEE Trans. Acoust. Speech Signal Process.*, vol. 28, no. 4, pp. 454–467, Aug. 1980, doi: 10.1109/TASSP.1980.1163430.

[24] S. D. Snyder and C. H. Hansen, "The effect of transfer function estimation errors on the filtered-x LMS algorithm," *IEEE Trans. Signal Process.*, vol. 42, no. 4, pp. 950–953, Apr. 1994, doi: 10.1109/78.285659.

[25] S. Ogasawara and H. Akagi, "Suppression of common-mode voltage in a PWM rectifier/inverter system," in *Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248)*, Chicago, IL, USA: IEEE, 2001, pp. 2015–2021. doi: 10.1109/IAS.2001.955904.

[26] R. Kebel, "Predicting Conducted EMI of an Inverter Driven Aircraft's Electric Power Train — Symmetry and Network Type," in *2022 ESA Workshop on Aerospace EMC (Aerospace EMC)*, Virtual: IEEE, May 2022, pp. 01–06. doi: 10.23919/AerospaceEMC54301.2022.9828555.

[27] "Identify discrete-time filter parameters from frequency response data - MATLAB invfreqz." The MathWorks, Inc. Accessed: Nov. 03, 2023. [Online]. Available: https://de.mathworks.com/help/signal/ref/invfreqz.html?searchHighlight=invfreqz&s_tid=srchtitle_invfreqz_1

[28] A. A. Khan and K. K. Dey, *A first course in electronics*. New Delhi: PHI Learning Private Limited, 2009.

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