Frequency-Selective Reduction of Power Electronic Switching Noise by Applying Synthesized Gate Signals

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***Abstract*—The high-frequency switching of power transistors in electronic systems can be a significant source of electromagnetic emissions (EMI). Simple measures like reducing the high-frequency disturbances by introducing an additional gate resistor lead to an increase of the switching losses. This creates a conflict of interests between the reduction of disturbances and high system efficiency. More complex active gate drivers offers improved compromises between EMI and efficiency. Avoiding steep switching slopes, overshoots or sharp edges are typical measures. The whole spectrum is modified this way and efficiency is still affected. In many cases, only a narrow banded modification of the spectrum might be needed to avoid the excitation of critical system resonances. This can be reached by a target signal-oriented control of the gate of the transistors. In the target signal the critical RF components should be reduced. Maximum control of the target signal is possible with fully synthesized gate signals. The reduction of some harmonics in the switching spectrum may lead to overshoots in time domain due to the Gibbs phenomenon. These overshoots may violate the physical limits of a transistor and cannot be realized. In this work, a method is presented to determine the target signal considering all physical limits. The found approach is applied in simulation to the signal of the drain-source voltage of a boost converter to reduce the harmonics in the FM broadcasting range. The gate control signal is determined for this application.**

Keywords—power electronics, active gate driving, constraint-satisfaction problem, electromagnetic compatibility

I. Introduction

Power electronic systems can be a significant source of **e**lectro**m**agnetic **i**nterferences (EMI) due to the high-frequency switching of power transistors. Different approaches are known to reduce these disturbances. Passive filters are a frequently used solution. These attenuate the generated disturbances. Despite their effectiveness, passive filters tend to be expensive, heavy and bulky. Instead of attenuating already generated disturbances, their creation can be reduced or avoided at their source of appearance. The switching transistors as EMI sources are controllable devices. Therefore, the EMI can be reduced by using appropriate gate drivers.

Typically, conventional gate drivers are used to control the transistors. These have the task to turn the transistors on or off quickly and minimize the switching losses. Steep slopes usually create overshoots, oscillations and other high-frequency disturbances. Slowing down the switching slope reduces these disturbances. This can be realized by adding an additional gate resistance. The switching behavior is improved regarding EMI, but the power losses are increased. This conflict between the reduction of EMI and the increase of power losses has to be optimized.

Active **g**ate **d**rivers (AGD) use more sophisticated methods to control the switching behavior of the transistor. As a result, steep switching slopes with less oscillations and overshoots can be realized. Hereby, a better compromise between EMI and efficiency can be achieved. There are different approaches in AGDs to control the gate. The most frequently used methods are the adaption of the gate-resistance ([1] and [2]), the adaption of the input capacitance [3], the adaption of the gate-current ([4] and [5]) or the adaption of the gate-voltage ([6] and [7]). A schematic illustration of these strategies is given in Fig. 1. The switching pattern generated by the voltage source, current source, variable gate-resistances or variable input capacitances are determined in the control unit. The determination of the switching pattern is divided into two steps. At first, the target signal (e.g. the desired drain-source voltage waveform) has to be determined. At the second step, the required gate control signal is calculated. Here, e.g., simulated annealing [8] or particle-swarm optimization algorithms [9] or neural networks [10] are used.

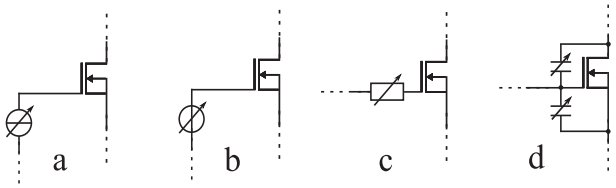

Fig. 1:Schematics of different active gate driving strategies with (a) a controlled current source, (b) a controlled voltage source, (c) an additional variable gate resistance and (d) variable external capacitances

To illustrate this, the time- and frequency-domain signals of Fig. 2 are discussed now. As an example, a trapezoidal switching waveform with steep slopes is considered, the disturbances in the FM broadcasting range exceed a given limit by 20 dB and have to be reduced by this value. As mentioned before, the reduction can be done by flattening the switching slope, as depicted in Fig. 2 in yellow. In this case, the whole spectrum of the switching waveform is influenced to fulfill the limits given in EMC standards, e.g., CISPR 25 [11] in automotive. By doing so, the whole spectrum of the critical signal is influenced. Amplitudes of high-frequency signal components are reduced and the switching power losses are increased. Another approach is to reduce the amplitudes selectively only for the specific frequency range. This way steep switching slopes can be maintained and therefore a high efficiency. The resulting signal is shown in Fig. 2 in blue. The appropriate control signal can be found by an optimization

method. However, another problem occurs. The Gibbs phenomenon causes new "oscillations" that cannot be generated by the strongly nonlinear power electronic system. So, not any arbitrarily given target signal can be realized, for some signals control signals do not exist. These limitations must be considered by the optimization strategy to find a control signal that respects the system's limits. The problem of finding physical signals is solved by extending the optimization methods this way that important constraints can be considered.

In this work, the target signal is given in frequency domain. A frequency-selective reduction of amplitudes is performed to satisfy EMC standards. The target signal may violate physical limitations using this approach. Therefore, the physical limitations of the switching waveform are analyzed. A method to adjust the target signal to meet the limitations is described. An arbitrary signal results that has to be generated. Therefore, a maximum flexible AGD is necessary. This can be realized by a high bandwidth signal synthesizer, e.g., an **a**rbitrary **w**aveform **g**enerator (AWG), with high power output. That can be achieved with a high bandwidth power amplifier. The system can freely generate control signals and is presented in [12]. With the help of optimization algorithms appropriate control signals can be found.

A detailed description of this method to determine a physical target signal is given in section II. The application of this theory and the transfer to an AGD for a boost converter is given in section III. A conclusion and outlook close this work.

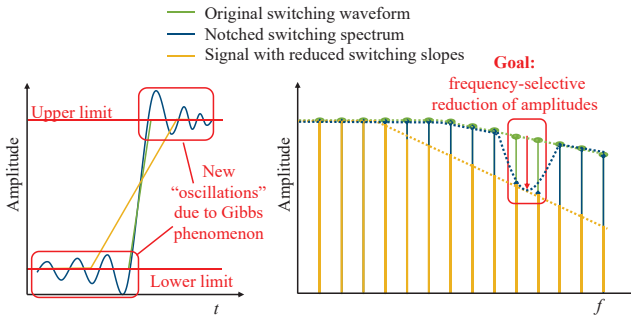

Fig. 2: Trapezoidal signal, notched signal and signal with reduced switching slopes in time (left) and frequency (right) domain

II. Theory

In the following, the control signal-finding problem is discussed for a generic switching cell as fundamental building block of power electronic systems. To find the signal, a generic description of a constraint-satisfaction-problem is given and applied to the switching cell. Furthermore, the proposed heuristic optimization algorithm to determine the necessary gate control signal is presented.

A. Generic Switching Cell

Switching transistors are the main functional component of power electronic systems. The building block of power electronic systems are the switching cells in Fig. 3. The buffer capacitor C is used to stabilize the voltage at these terminals. A half bridge with two transistors is shown in Fig. 3 on the left. In Fig. 3 in the middle, a switching cell consisting of a high side transistor and a diode in the low-side path is depicted. In Fig. 3 in the right, a switching cell with a diode in the high-side path and a low-side transistor is shown. In the following, the drain-source voltage v_{ds} is considered as target signal.

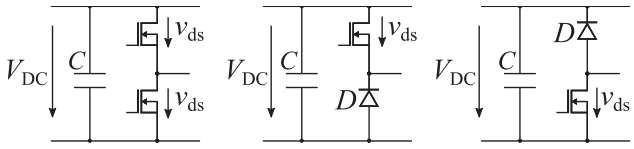

Fig. 3: Schematics of generic switching cells

B. Phyiscal Limitations for the Switching Waveforms

The controllable range of the drain-source voltage v_{ds} is limited by the output behavior of the transistor of the switching cell. In the conducting state the behavior can be described with the drain-source resistance R_{ds}. If a high voltage is applied to the gate, R_{ds} is equal to the on-resistance $R_{\mathrm{ds,on}}$. The voltage drop $V_{\mathrm{ds,low}}$ is near to zero. If the gate voltage is zero, the transistor is turned off. In this case, the drain-source voltage $V_{\mathrm{ds,high}}$ is defined by the voltage between drain and source, i.e. the voltage of the stabilizing capacitance. Therefore, v_{ds} is limited by $V_{\mathrm{ds,low}}$ and $V_{\mathrm{ds,high}}$. This is depicted in Fig. 4 by lines. As mentioned before, the frequency-selective narrow-band reduction of disturbances may offer the potential to reduce the conflict of interests between EMI and efficiency, but due to Gibbs phenomenon, oscillations, as shown in Fig. 4, have to be generated that are outside of the transistors voltage range. A target signal $v_{\mathrm{ds,t}}$ is needed that is located in the controllable range and generates the spectrum with frequency-selective reduced (notched) amplitudes. In [13], this is done by a DC-offset but this causes higher power losses when the transistor is conducting. The goal of minimal power losses cannot be reached this way. To solve this problem, the adaption of the spectrum is done by solving a constraint-satisfaction-problem in this work.

C. Generic Description of a Constraint-Satisfaction-Problem

The aim of a **c**onstraint-**s**atisfaction-**p**roblem (CSP) is to express a problem as a set of l variables and a set of m constraints on these variables. In general, a CSP describes a combinatoric problem that is defined by a quadruplet (X, D, C, R) with

$$X = \{X_1, X_2, \dots, X_{\mathrm{l}}\} \tag{1}$$

$$D = \{D_1, D_2, \dots, D_{\mathrm{l}}\} \tag{2}$$

$$C = \{C_1, C_2, \dots, C_{\mathrm{m}}\} \tag{3}$$

$$R = \{R_1, R_2, \dots, R_{\mathrm{m}}\}. \tag{4}$$

The quantity X is a set of variables. The range of the variables is defined by the set of domains D, where D_{i} is the set of possible values of X_{i}. The quantity C is the set of constraints of the variables X. The permitted combinations of values are defined by a set of relations R. Thereby, the relation R_{i} corresponding to C_{i} is defined by the Cartesian product $D_{\mathrm{i1}} \times D_{\mathrm{i2}} \times D_{\mathrm{id}}$ of the domains of the d involved variables. A solution of a CSP is found if a value for each variable of its domain is found which satisfies all constraints. Search algorithms can be used to solve the CSP. Commonly applied algorithms are tree search algorithms like backtracking. [14]

D. *Transfer of the Constraint-Satisfaction-Problem to the Generic Switching Cell to Find the Needed Switching Waveform*

In this section, the CSP theory is applied. The aim is to find a signal that attenuates EMI in a given frequency band and considers the physical limits of the observed power electronic system. The previously described switching cell is considered. The drain-source voltage v_{ds} is the signal to be optimized. An exemplary disturbing signal, v_{ds}, is shown in Fig. 4 in time and frequency domain that should be reduced by 20 dB in the frequency range from 76 MHz-108 MHz. As discussed before, the notched spectrum cannot be realized by the transistor circuit.

For optimization the periodic signal is represented by a Fourier-series:

$$v_{\mathrm{ds}} = \frac{a_0}{2} + \sum_{k=1}^{\infty} a_k \cos(2\pi f_0 k t) + b_k \sin(2\pi f_0 k t) \qquad (5)$$

with a_k and b_k as coefficients of the Fourier series, f_0 as fundamental frequency and t as time.

The set of variables X of the CSP are the a_k and b_k of the Fourier series. The constraints of this problem can be expressed by

$$C_1 : v_{\mathrm{ds}}(X) - V_{\mathrm{ds,high}} \leq 0 \qquad (6)$$

$$C_2 : V_{\mathrm{ds,low}} - v_{\mathrm{ds}}(X) \leq 0 \qquad (7)$$

$$C_{3\ldots\mathrm{m}} : X_{\mathrm{notch},1\ldots\mathrm{m}-3} - A_{\mathrm{notch},1\ldots\mathrm{m}-3} = 0 \qquad (8)$$

with m the total number of constraints. The variables $X_{\mathrm{notch},1\ldots\mathrm{m}-3}$ correspond to the a_k and b_k of the frequencies that should be reduced and $A_{\mathrm{notch},1\ldots\mathrm{m}-3}$ are the corresponding amplitudes to the $X_{\mathrm{notch},1\ldots\mathrm{m}-3}$. It is possible to define more constraints that have to be fulfilled by the signal. E.g., the amplitudes of high-frequency harmonics should not be influenced to avoid additional high frequency disturbances.

As mentioned before, the CSP is usually solved by the application of a tree search algorithm like backtracking. The usage of such an algorithm may be a good choice if the set of domains D in Eq. (2) only contains a few discrete states. However, the set of domains D contains infinite states in the considered application. Therefore, the usage of a backtracking algorithm is not feasible. Thus, a modification of a constrained minimization problem is used. The objective function to be minimized is set to a constant function of zero $f(X) = 0$. Hence, only the constraints have to be satisfied, which corresponds to solving a CSP. There is only a solution if all constraints are satisfied. The optimization problem can be written in general as

$$\begin{aligned} &\min_X f(X) \\ &s.t. \\ &\quad h_{\mathrm{i}}(X) \leq 0, \mathrm{i} = 1, 2, \ldots, p \\ &\quad g_{\mathrm{j}}(X) =, \mathrm{j} = 1, 2, \ldots, q \end{aligned} \qquad (9)$$

with $h_{\mathrm{i}}(x)$ the p inequality constraints and $g_{\mathrm{j}}(x)$ the q equality constraints. Here, the inequality constraints are C_1 in Eq. (6) and C_2 in Eq. (7), and the equality constraints are $C_{3\ldots\mathrm{m}}$ in Eq. (8). The optimization problem of Eq. (9) is solved using an interior-point algorithm as implemented in MATLAB with the function "fmincon" used here. The resulting signal that satisfies all constraints is depicted in Fig. 4 in green. In addition, the constraints (6) to (8) are graphically illustrated in Fig. 4.

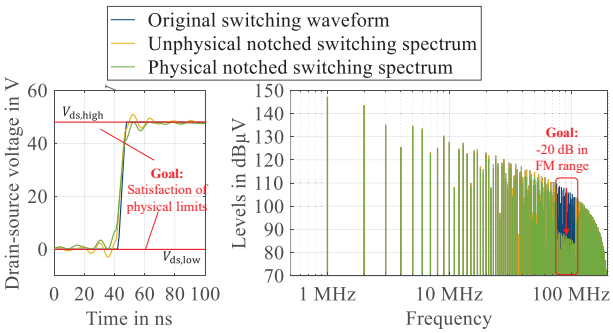

Fig. 4: Original drain-source voltage and notched signal with and without violations of physical limitations

E. *Determination of the required gate control signal*

The proposed method to determine the required gate control signal to generate the previously calculated target signal of the drain-source voltage is explained in this section. As mentioned before, the previous approaches of active gate driving deal with an optimization in time domain. In this work, an optimization in frequency domain is performed. The gate control signal is represented by a Fourier series according to (10)

$$v_{\mathrm{cntrl}} = \frac{a_{\mathrm{c},0}}{2} + \sum_{k=1}^{\infty} a_{\mathrm{c},k} \cos(2\pi f_0 k t) + b_{\mathrm{c},k} \sin(2\pi f_0 k t)\,. \qquad (10)$$

The goal of the algorithm is to find the appropriate coefficients $a_{\mathrm{c},0}$, $a_{\mathrm{c},k}$ and $b_{\mathrm{c},k}$ for the gate control signal to achieve the desired switching behavior. A heuristic search algorithm is used to find the right coefficients. This approach is similar to the optimization in [12], but here it is applied to the Fourier coefficients (frequency domain) and not to the amplitudes of step functions (time domain). By adjusting the Fourier coefficients, the gate control signal is varied for the whole switching period. If a better control signal is found, this signal is taken as the starting point for the next random variation. In each iteration, the range in which the coefficients of the Fourier series are randomly varied is reduced. This should enable the convergence of the algorithm while avoiding local minima. The flowchart in Fig. 5 shows the general procedure. At the beginning, all variables are initialized, and the target control signal is determined as described before. As a starting point for the optimization a trapezoidal PWM signal with the necessary duty cycle is used. During the variation phase, the coefficients of the Fourier series in (10) are modified by adding a random number $x_{\mathrm{rand},k}$ in the range [-1,1]. On one hand, this random number is weighted by the factor $A_{\mathrm{var,n}}$ in the n-th iteration, which is a decreasing series to enable the convergence of the optimization. On the other hand, $x_{\mathrm{rand},k}$ is weighted with the factor LP_k that generates a low-pass filtering of the variables for the variation of the coefficients because a wide variation of high-order harmonics is not expected to be required. So, the variation of the coefficients of the Fourier series is performed by equation (11):

$$a_{\mathrm{var},k} = x_{\mathrm{rand},k} \cdot A_{\mathrm{var,n}} \cdot LP_k \tag{11}$$

and analogously for $a_{\mathrm{var},0}$ and $b_{\mathrm{var},k}$. Therefore, the control signal to be tested is determined by

$$\begin{aligned} v_{\mathrm{cntrl,test}} &= \frac{a_{\mathrm{c},0} + a_{\mathrm{var},0}}{2} \\ &+ \sum_{k=1}^{\infty} [(a_{\mathrm{c},k} + a_{\mathrm{var},k}) \cos(2\pi f_0 kt) \\ &+ (b_{\mathrm{c},k} + b_{\mathrm{var},k}) \sin(2\pi f_0 kt)]. \end{aligned} \tag{12}$$

The test signal is applied to the amplifier that is connected to the gate of the transistor. The resulting drain-source voltage is measured. After that, the mean squared error e_{n} of the n-th iteration between the measured signal $v_{\mathrm{ds,m}}$ and the target signal $v_{\mathrm{ds,t}}$ is calculated by equation (13):

$$e_{\mathrm{n}} = \overline{\left(v_{\mathrm{ds,m}} - v_{\mathrm{ds,t}}\right)^2}. \tag{13}$$

If e_{n} is smaller than e_{best}, the last tested coefficients $(a_{\mathrm{c},k} + a_{\mathrm{var},k})$ and $(b_{\mathrm{c},k} + b_{\mathrm{var},k})$ becomes the new $a_{\mathrm{c},k}$ and $b_{\mathrm{c},k}$ respectively. Analogous, e_{n} becomes the new e_{best}. If e_{n} is higher than e_{best} the actually tested coefficients are discarded. Then, the iteration counter n is increased. The optimization process is repeated until the maximal number of iterations $\mathrm{n_{max}}$ is reached.

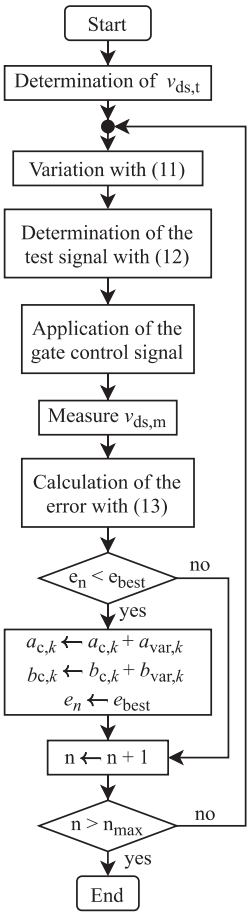

Fig. 5: Flowchart of the heuristic optimization algorithm to determine the gate control signal

III. Simulatory Demonstration

In this section, the previously described theory is applied to a simulation model in MATLAB/Simulink. Here, in particular Simscape is used. A boost converter is taken into consideration. Here, the goal is to reduce the amplitudes in the FM broadcasting range (i.e. 76 MHz-108 MHz) by 20 dB. The required drain-source voltage that satisfies all constraints is determined. The necessary gate control signal is found to generate the target $v_{\mathrm{ds,t}}$. The results are discussed and compared to other approaches.

A. Test Setup

A boost converter is considered as the test system. The schematic is shown in Fig. 6. An input voltage V_{in} of 12 V is converted to an output voltage V_{out} of 48 V. At the input a buffer capacitor C_{in} and storage choke L are used. The topology of Fig. 3 with a low-side transistor and a high-side diode is used as the switching cell. In addition, a parasitic gate-source C_{gs}, gate-drain C_{gd} and drain-source C_{ds} capacitance and the body diode are considered. Furthermore, parasitic lead inductances L_1 to L_3 are respected. Thus, damped oscillations at the end of the switching slopes arise in the drain-source voltage, as shown in Fig. 8 in blue. A buffer capacitor C_{out} and a load resistance R_{L} are connected to the output. In the following, the simplified schematic of the boost converter of Fig. 7 is taken into consideration. Due to the large storage elements (input capacitance and inductance, output capacitance), the circuit has a large settling time. Therefore, a long simulation time is needed since the boost converter is to be considered in steady state. By replacing the large storage elements, the settling time is widely reduced leading to much shorter simulation time. The input to the switching cell, marked in yellow, is modeled by a constant current source. The switching cell marked in blue and the gate driving circuit marked in green are not modified. A constant voltage source and a resistor model the output capacitor and the load resistance marked in red.

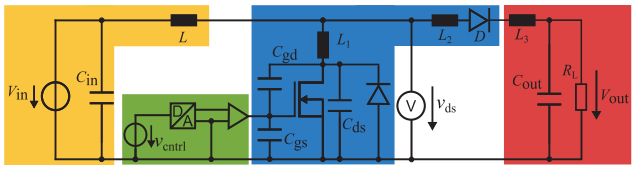

Fig. 6: Schematic of a boost converter

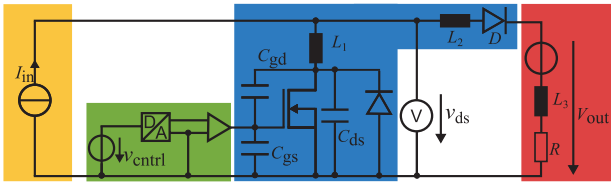

Fig. 7: Simplified schematic of a boost converter for time efficient simulations

B. Goal

The goal is a frequency-selective reduction of the spectrum of the drain-source voltage. A target spectrum has to be generated. In this example, the amplitudes in FM broadcasting range should be reduced by 20 dB. The amplitudes of the frequency range from 76 MHz up to 108 MHz are influenced. The drain-source voltage v_{ds} is shown in Fig. 8 in blue using a trapezoidal gate control signal. The depicted signal is determined by simulation results. If the amplitudes of this signal are reduced by 20 dB in FM range, the yellow spectrum in Fig. 8 on the right results. As described before, this requirement may violate physical limitations as shown in Fig. 8 in yellow on the left. Therefore, a physical

signal should be found that satisfies the emission constraints in the FM broadcasting range and meets all physical limitations. This is done by the application of solving a CSP on this issue. This is described in the following.

C. Calculation of a Required Drain-Source Voltage Waveform

The disturbed drain-source voltage v_{ds} shown in Fig. 8 in blue is taken into consideration. The maximum of v_{ds} is limited by the constant voltage in cutoff region. So, $V_{\mathrm{ds,high}}$ is set to the value of 49.8 V in this case. The minimum of v_{ds} is given by the minimal $R_{\mathrm{ds,on}}$ and the drain current during the MOSFET is interconnected. In this example, $V_{\mathrm{ds,low}}$ equals approximately 0.3 V. As previously described, the amplitudes in the FM broadcasting range should to be reduced by 20 dB applying a Tukey window. The yellow graph on the left of Fig. 8 shows the results for the time-domain signal if the reduction of the amplitudes is performed (without considering further constraints). These signals violate the upper and lower limits of the drain-source voltage. 33 harmonics have to be influenced. Therefore, 66 variables of the CSP are influenced because of the representation by the Fourier series. The constants A_{FM} are defined by the corresponding variables in the disturbed case X_{FM}. Considering the required reduction, $A_{\mathrm{FM,dB}} = X_{\mathrm{FM,dB}} - 20\,\mathrm{dB}$ results. The change of amplitudes of high-frequency signal components is prohibited to avoid the increase of undesired high-frequency disturbances (this constraint is freely chosen). The constraints can be formulated in summary by

$$C_1 \colon v_{\mathrm{ds}}(X) - 49.8\,\mathrm{V} \leq 0 \tag{14}$$

$$C_2 \colon 0.3\,\mathrm{V} - v_{\mathrm{ds}}(X) \leq 0 \tag{15}$$

$$C_{3\ldots69} \colon X_{\mathrm{FM},1\ldots66} - A_{\mathrm{FM},1\ldots66} = 0 \tag{16}$$

$$C_{70\ldots\mathrm{m}} \colon X_{\mathrm{HF},1\ldots\mathrm{m}-70} - A_{\mathrm{HF},1\ldots\mathrm{m}-70} = 0 \tag{17}$$

with $A_{\mathrm{HF},1\ldots\mathrm{m}-70}$ as the amplitudes of the corresponding disturbed signal. The green graph is calculated by solving the CSP as described in section II.D and satisfies all constraints in time and frequency domain as depicted. Differences to the original signal appears in the physically notched switching spectrum in the surrounding area to the notched range to satisfy the physical upper and lower limit.

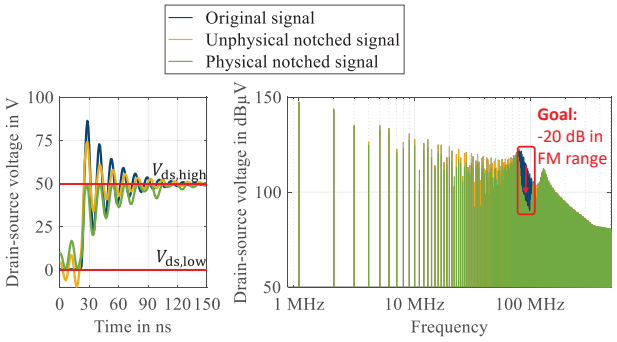

Fig. 8: Original, unphysically and physically notched drain-source voltage

D. Calculation of the Necessary Gate-Control Voltage Waveform

The determination of the necessary gate-control signal to generate the previous calculated target drain-source voltage shown in Fig. 8 in green is performed using the heuristic search approach of II.E. Here, the variable A_{var} is a decreasing vector of n = 1000 elements in the range $[10^{-2}, 10^{-3}]$ and LP is a low-pass filter with a bandwidth of 60 MHz and a drop of -60 dB/decade. The resulting necessary gate control signal is shown in Fig. 9.

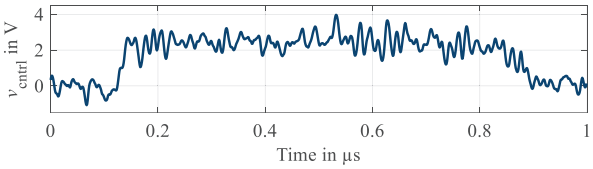

Fig. 9: Determined gate control signal

E. Discussion of the Results

The previously determined gate control signal is applied to the gate of the MOSFET of the investigated boost converter. The simulation result of the drain-source voltage is shown in Fig. 10 in comparison to the target v_{ds}. A sufficient match can be observed. As mentioned before, the efficiency of the switching slope is an important parameter of power electronic systems. Using conventional gate driver, the transistor is totally cutoff and conducting. Therefore, the power losses in cutoff and conduction state are minimized. The power losses are depicted in Fig. 12. The average power losses are 3.7 W. Generating the target v_{ds}, the average power losses are increased to approximately 12.1 W. The power losses of the notched signal are also shown in Fig. 12. It can be seen that the power losses in cutoff and conducting state are more increased because of the remaining oscillations. Therefore, the transistor is not totally cutoff and conducting.

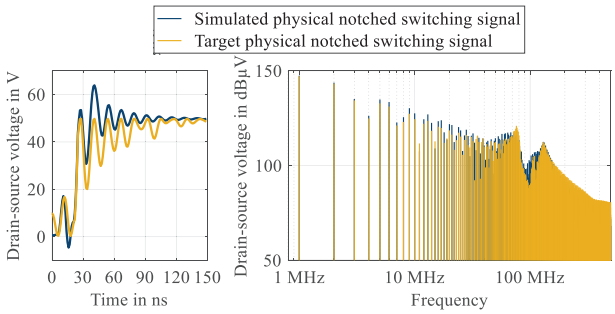

Fig. 10: Simulated and target drain-source voltage

F. Comparison to Previous Approaches

Commonly used approaches to satisfy EMC requirements of a switched transistor are the reduction of the switching slope of the gate control signal. This can be realized with an additional gate resistance, as described before. Also here, a reduction of 20 dB is requested in the FM range for this signal. To do so, the slopes of the gate control have to be reduced to 160 ns. The simulated time and frequency domain signals of the drain-source voltage are shown in Fig. 11. Just like notching the original signal of the switched MOSFET, a reduction of 20 dB in FM range is reached. However, when looking at the power losses in Fig. 12, it can be seen that the switching losses increase. The average power losses are 13.7 W. Applying the approach of notching the spectrum, the switching losses can be reduced by 1.6 W compared to lowering the switching slope, but the losses in the conducting and cutoff state arises, as previously described.

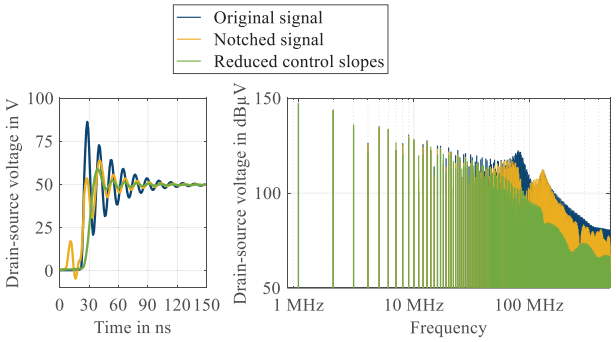

Fig. 11: Original and notched drain-source voltage and v_{ds} with reduced control slopes

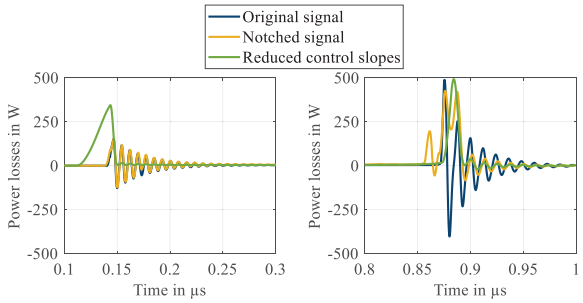

Fig. 12: Power losses of the original and notched signal and the signal with reduced control slopes

IV. Conclusion and Outlook

Power electronic systems are potential sources of electromagnetic disturbances. A reduction of these disturbances usually results in a degradation of the efficiency. Methods of active gate driving are used to influence the switching behavior of transistors to optimize this conflict of objectives. The aim of most of these approaches is to track a reference signal. In this work, a method was presented to frequency-selective reduce the amplitudes of a disturbed signal. Here, the drain-source voltage of a boost converter was considered as the signal to be optimized. In power electronic circuits, the physical limits of the drain-source voltage can be violated because of the Gibbs phenomenon if harmonics are selectively altered. Therefore, a method was described to determine a reference signal that satisfies all constraints. A constraint-satisfaction-problem is solved to handle this task. This approach was applied to reduce the amplitudes of the drain-source voltage of a boost converter in the FM broadcasting range by 20 dB. The average power losses are strongly increased using conventional methods to fulfill this requirement. Applying the proposed method of notching the spectrum, the average power losses are less increased (here by 1.6 W, i.e. 1.1 % of the transfer power of 144 W). This offers a great potential for the optimization of power electronic systems.

This method is the foundation to determine the reference signal for active gate driving if modifications of the spectrum are undertaken. In a future work, the approach should be applied to a laboratory test system of a boost converter to illustrate the benefits of selective frequency notching using a more performant AGD method. A method of active gate driving should be used to reduce high-frequency disturbances. The quality of this approaches should be validated by a measurement of the remaining disturbances at an artificial network.

References

[1] C. P. Dymond, J. Wang, D. Liu, J. J. O. Dalton, N. McNeill, D. Pamunuwa, S. J. Hollis and B. H. Stark, “A 6.7-GHz active gate driver for GaN FETs to combat overshoot, ringing, and EMI,” *IEEE Trans. Power Electronics,* vol. 33, no. 1, pp. 581-594, Jan. 2018.

[2] Paredes, V. Sala, H. Ghorbani and L. Romeral, “A novel active gate driver for silicon carbide MOSFET,” *IECON 2016 – 42nd Annual Conference of the IEEE Industrial Electronics Society*, pp. 3172-3177

[3] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, H.A. Mantooth, “A Review on Switching Slew Rate Control for Silicon Carbide Devices using Active Gate Drivers,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Early Access, pp. 1-18, July 2020.

[4] M. V. Krishna and K. Hatua, “Closed loop analog active gate driver for fast switching and active damping of SiC MOSFET,” *2018 IEEE Appl. Power Electron. Conf. and Exposition (APEC)*, pp. 3017-3021.

[5] V. Subotskaya, B. Deutschmann, “Adaptive current source driver for high-frequency boost converter to reduce EMI generation,“ *Conference on Ph. D. Research in Microelectronics and Electronics, Institute of Electrical and Electronics Engineers et al. 2017 – PRIME 2017*, pp. 333-336.

[6] C. Krause, A. Bendicks, T. D¨orlemann, and S. Frei, ″Synthesis of an optimized control signal for an improved EMC switching behavior of MOSFETs Using a System Characterization Approach,″ in *Proc. Int. Symp. Electromagn. Compat. Eur*., Barcelona, Spain, 2-6 Sep. 2019, pp. 345-350.

[7] C. Krause, A. Bendicks, and S. Frei, ″Verbesserung des EMV-Verhaltens getakteter MOSFETs mithilfe synthetisierter Ansteuerungssignale auf Grundlage einer Netzwerkanalyse und des EKV-Modells,″ in *Proc. Conf. Electromagn. Compat*., Cologne, Germany, 12-13 May 2020, pp. 131-138.

[8] K. Miyazaki, S. Abe, M. Tsukuda, I. Omura, K. Wada, M. Takamiya, T. Sakurai, “General-Purpose Clocked Gate Driver IC With Programmable 63-Level Drivability to Optimize Overshoot and Energy Loss in Switching by a Simulated Annealing Algorithm,“ *IEEE Trans. on Ind. Applicat.*, vol. 53, no. 3, pp. 2350-2357, May/June 2017.

[9] Y.S. Cheng, T. Mannen, K. Wada, K. Miyazaki, M. Koutarou, T. Sakurai, “Optimization Platform to Find a Switching Pattern of Digital Active Gate Drive for Reducing Both Switching Loss and Surge Voltage,“ *IEEE Trans. on Ind. Applicat.,* vol. 55, no. 5, pp. 5023-5031 September/October 2019.

[10] X. Zeng, Z. Li, J. Wan, J. Zhang, M. Ren, W. Gao, Z. Li, B. Zhang, “Embedded Hardware Artificial Neural Network Control for Global and Real-Time Imbalance Current Suppression of Parallel Connected IGBTs,“ *IEEE Trans. Ind. Electron*., vol. 67, no. 3, pp. 2186-2196, March 2020.

[11] CISPR 25 –Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers,” Ed.4.0, 2015.

[12] C. Krause, A. Bendicks and S. Frei, “Active gate control with synthesized signals to avoide overshoots and ringing in DC-to-Dc converters,” *PCIM Europe 2021*, Nuremberg, Germany, 03-07 May 2021, pp.1256-1262.

[13] T. Dörlemann, A. Bendicks, C. Krause and S. Frei, “Noise reduction in periodically switching MOSFET circuits using iteratively found synthesized control signals”. in in *Proc. Int. Symp. Electromagn. Compat. Eur*., Barcelona, Spain, 2-6 Sep. 2019, pp. 848-853.

[14] K. Ghédira, *Constraint satisfaction problems*, London; Hoboken, N.J.: ISTE; Wiley, 2013.