Wide-Frequency EMI Suppression of Stationary Clocked Systems by Injecting Successively Adapted Cancellation Signals

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***Abstract*—Active cancellation can suppress electromagnetic interference (EMI) of clocked systems like power electronic converters. Considering clocked systems that operate stationary over a sufficient time, there are stable harmonics that can be individually suppressed by destructive sine waves. These sine waves can be superposed to create a synthesized wide bandwidth cancellation signal. Adaptive approaches have proven to be very effective to find the right parameters for each sine wave. Bothersome effects, like complex frequency characteristics or delays, can be compensated by appropriate amplitudes and phases. Therefore, this method does not suffer from the same limitations as active techniques with feedback- or feedforward-topologies. If the disturbances are constant over a sufficient time, the parameters for the cancelling sine waves can be found simultaneously or successively. Until now, only the first option has been shown with an adaptive cancelling FPGA system. Since the cancelling logic needed to be implemented for each cancelling sine wave and the resources of any FPGA are limited, the number of suppressible harmonics was limited as well. In this work, this limitation is resolved by a successive approach that enables the application of the method to a very large number of harmonics. The fundamental theory is discussed, and a robust algorithm is presented. A cancellation system is realized and applied to a 48V/12V DC/DC converter (e.g. for automotive applications) to suppress the frequency range of 150 kHz to 30 MHz in regard to the automotive EMC standard CISPR 25.**

Keywords—DC/DC Converter; EMI; Suppression; Synthesized Signals; FPGA

I. INTRODUCTION

Clocked systems (and especially switching power electronics) tend to be considerable sources of EMI. To comply with international standards (e.g. [1] in automotive), the EMI is commonly reduced by the application of passive filters or shields that are often bulky, heavy and expensive. Another strategy is the active cancellation of disturbing signals by a destructive interference between noise and anti-noise [2]. This strategy is applied commonly in acoustics and successively in EMC.

For EMC, active EMI filters have been introduced in [3], elaborated on in [4]-[6], and further generalized and analyzed in [7] and [8]. Like passive EMI filters, active filters are connected between the noise source and the sink. Active filters can be classified as feedforward- or feedback-types. In feedforward active filters, the disturbances are measured at the noise source, processed and injected back into the system to achieve a destructive interference between noise and anti-noise. Feedback active filters utilize a control loop to minimize the disturbances at the sink; again, the anti-noise is generated from a measured signal. As all analog or digital circuitry introduces an inevitable delay, noise and anti-noise can never be exactly simultaneous. Hence, the achievable EMI reduction and the suppressible frequency range are limited for active filters as analyzed in [9]. To resolve the issue of a systematically delayed signal path, the cancellation signal can be artificially synthesized and applied synchronously with the disturbances [9], [10]. Remaining transfer functions are compensated by the shape of the synthesized signal improving the cancellation's effectivity widely. This strategy performs especially well for periodic disturbances. Some periods may be needed to find the cancellation signal, but afterwards a very high noise suppression can be achieved during stationary operation. Furthermore, the compensation signal can be constructed from harmonic sine waves by fast and robust algorithms.

In [9], a self-adapting algorithm was transferred from (acoustical) Active Noise Control (ANC) to EMC. The algorithm was implemented on an FPGA system with fast Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) and applied to the first six harmonics of a DC/DC converter. By doing so, the frequency ranges of long wave (LW, 150 kHz-300 kHz) and medium wave (MW, 530 kHz-1.8 MHz) were suppressed in regard to the automotive standard CISPR 25 [1]. The algorithm was implemented separately for each considered harmonic enabling a simultaneous optimization. Due to this resource-heavy implementation on the experimental FPGA system, only a small number of harmonics could be suppressed.

To resolve this issue, an external trainer was introduced and successfully applied in [10]. This external trainer found and synthesized the necessary cancellation signal and passed it to the FPGA (with DAC) that was used as an arbitrary waveform generator. By applying this system to a DC/DC converter, the complete frequency range of 150 kHz to 30 MHz was suppressed. Since the external trainer is removed after training, the cancellation system must be taught for all relevant operating modes (and therefore disturbances) of the disturbing system. This cancellation system cannot independently adapt itself during operation.

In this work, an extension for the algorithm of [9] is developed that enables the FPGA to successively adapt to an arbitrary

number of harmonics. This system is independent from an external trainer and can adapt itself to, e.g., changed configurations of the system. At first, the fundamental theory of adapted harmonics cancellation is summarized and the idea of a successive signal generation is introduced. Then, the algorithm of [9] is presented in more detail and possible extensions for the successive signal generation are discussed. Afterward, the implemented algorithm is applied to a DC/DC converter over the frequency range of 150 kHz to 30 MHz. The cancellation system is presented and its effectivity is shown by measurements. A conclusion closes the work.

II. Theory

In this chapter, the fundamental theory of suppressing harmonics by artificial sine waves is briefly described. Afterward, the theory of successively generating cancellation signals is introduced.

A. Adapted Harmonics Cancellation

The fundamental concept of adapted harmonics cancellation [9] is illustrated in Figure 1. The clocked system is the source of disturbing harmonics that must be cancelled out. In this work, a DC/DC converter is considered as clocked system that creates harmonic disturbances due to the periodic switching of the transistors. The cancellation system is implemented on digital hardware and consists of an optimizer, a synthesizer, a DAC and an ADC. For cancellation, the synthesizer generates a sine wave for each disturbing harmonic. To find the right amplitudes and phases for the cancellation, an optimizer is utilized. The synchronization of the generated sine waves and the disturbing harmonics is maintained by a suitable synchronization signal. To link the clocked system and the cancellation system, interfaces are necessary. A sensor consisting of a sensing circuit and an ADC is used to measure the resulting disturbances. To couple the cancelling waveform into the clocked system, an injector is necessary. This injector consists of an injecting circuit and a DAC.

B. Successive Signal Generation

As stated before, much hardware resources are necessary if all considered harmonics are optimized simultaneously. To resolve this issue, the cancellation signal can be generated successively. At first, there is no cancellation signal and no disturbances are suppressed. Then, the first disturbing harmonic shall be suppressed. To do so, an optimizer finds the right amplitude and phase for the corresponding cancelling sine wave. Afterward, the second disturbing harmonic shall be suppressed. Again, the optimizer finds the correct parameters for the corresponding cancelling sine wave. By superposing the cancelling sine waves found by the optimizer, the cancellation signal is generated successively. This process can be repeated until all considered harmonics are suppressed. After the last harmonic, the process can start over again from the first harmonic. The previously synthesized cancellation signal can be adjusted to improve the result. Slow changes of the overall system (due to e.g. thermal drifts) can also be compensated this way.

III. FPGA Implementation

In this chapter, a possible FPGA implementation is developed for the theory depicted in II. At first, the adaptive notch

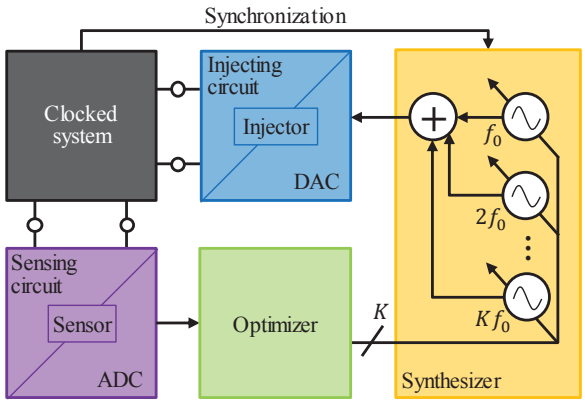

Figure 1: Concept of adapted harmonics cancellation

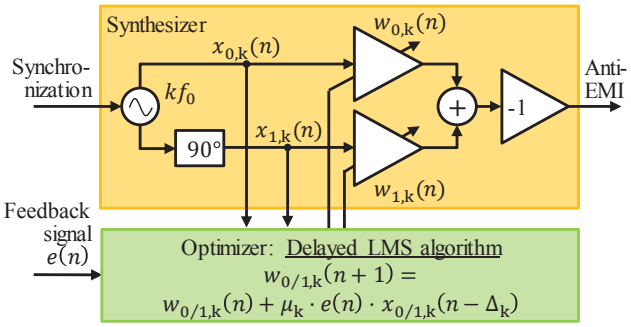

Figure 2: Structure of the adaptive notch filter

filter is introduced that is the base for the further developments. The stability of the algorithm is a very important aspect and is discussed in detail to derive necessary and possible extensions for the algorithm. Afterward, the extended algorithm is proposed.

A. Adaptive Notch Filter

In this work, the "single-frequency adaptive notch filter" developed in [11] and [12] is investigated. The fundamental structure is depicted in Figure 2. In this implementation, an arbitrary sine wave $x_{0,k}(n)$ with the frequency kf_0 is generated. This sine wave is triggered by a suitable synchronization signal. To adjust the sine wave's amplitude and phase, an orthogonal system is created by a phase-shift of 90° of the generated sine wave (or alternatively by an additional cosine wave). Both the original $x_{0,k}(n)$ and the phase-shifted signal $x_{1,k}(n)$ are respectively multiplied by the factors $w_{0,k}(n)$ and $w_{1,k}(n)$ and summated. Any sine wave with the frequency kf_0 can be created by adjusting these factors. The inversion is necessary for consistency with the optimization algorithm described in the following.

To find the optimum sine wave, the factors $w_{0,k}(n)$ and $w_{1,k}(n)$ are derived from the delayed LMS algorithm (note Figure 2) [13], [14]. This algorithm basically compares the error signal $e(n)$ with the generated signals $x_{0/1,k}(n)$ and adjusts the factors $w_{0/1,k}(n)$ to minimize the error. Note that the algorithm intrinsically optimizes only the harmonic that corresponds to the generated sine wave. So, an additional frequency selection, like filtering or FFTs, is not necessary for the error signal. For the stability of the algorithm, the signals must be correlated in time.

As DACs, ADCs and analog circuitries cause delays in the propagation of the signals, $e(n)$ is measured later than $x_{0/1,\mathrm{k}}(n)$ is generated. Therefore, the total delay Δ_k of the path from injecting to sensing must be respected in the update rule of the algorithm. The remaining variable μ_k is the step size of the algorithm. A large μ_k speeds up the convergence of the algorithm but may cause instability [15]. As there is a stationary operation of the system in this work, a very small μ_k is chosen for a precise adaption [16], [17].

B. Stability of the Delayed LMS Algorithm

As stated beforehand, the estimation of the total delay Δ_k of the path from injecting to sensing is critical for the stability of the algorithm. The error of this delay estimation can be translated to a phase error $\varphi_{\Delta,\mathrm{error,k}}$ for the respective harmonic k. In [18] and [19], it has been shown that phase errors of up to 40° do not slow down the convergence speed of the algorithm. But higher phase errors slow down the convergence of the algorithm significantly, and phase errors of 90° or greater cause the algorithm to be unstable. So, the phase error should be minimized for a quick and stable algorithm. If the target system is known, the delay Δ_k can be determined by, e.g., measurements beforehand. If the target system is unknown, the delay time must be found during operation. Here, a pragmatic approach is chosen in which different delay times are tested. Of course, the algorithm must detect if the delay time is correct or not. To identify a suitable criterion, simulated waveforms are discussed in the following.

In Figure 3, the simulated waveforms are depicted. The disturbance signal is a single harmonic that is eliminated by the found cancelling sine wave. The cancellation signal refers to the left axis, and the weights of the delayed LMS algorithm w_0 and w_1 refer to the right axis. Note the limited range of the cancellation signal due to the DAC's limits. Prior to applying this algorithm, it has to be ensured that the voltage range of the DAC is sufficient for the expected cancellation signal. For demonstration, four different phase errors (0°, 40°, 90°, 180°) are considered. Obviously, the algorithm converges after few periods for a phase error of 0°. For a phase error of 40°, the convergence speed is slightly reduced, but the algorithm is still quick and efficient. The LMS weights increase (or decrease) with only slight overshoots. For greater phase errors (here approximately 90°), the convergence speed is extremely reduced and the delayed LMS algorithm takes much longer to settle. The LMS weights oscillate and settle only after a long optimization time. For a phase error greater than 90° (here 180°), the algorithm becomes instable and the cancellation signal quickly reaches the limits of the DAC.

C. Extension for Successive Signal Generation

A flowchart for the successive signal generation is depicted in Figure 4. At the start, the first harmonic is selected and the delayed LMS algorithm is used to find the amplitude and phase for the corresponding cancelling sine wave. During optimization, the stability of the algorithm is checked. This can easily be done by checking if the cancellation signal reaches the DAC's limits or not. If the limits are reached, the algorithm is instable and the delay estimation Δ_k must be adjusted. Then, the optimization starts again for the new Δ_k. For each harmonic, the adaptive algorithm is given a defined time window to optimize the cancellation signal. Since the convergence can be quick (phase error below 40°) or slow (phase error above 40°), a sufficient amount of time must be chosen. After the optimization period,

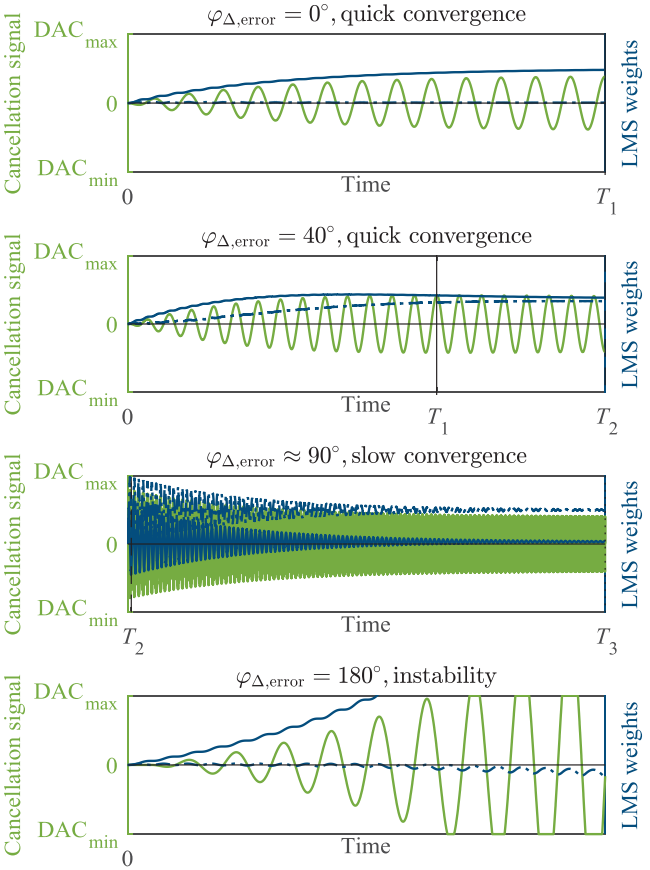

Figure 3: Simulated waveforms for the delayed LMS algorithm

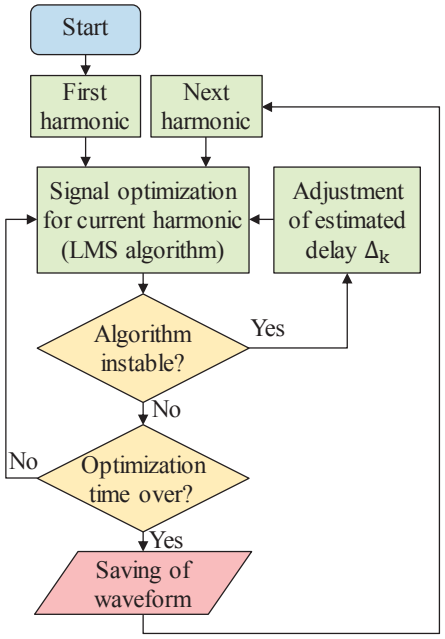

Figure 4: Flowchart for the successive signal generation

the resulting waveform (or the amplitude and phase information) is saved, and the cancellation signal is optimized for the next harmonic. By applying this procedure, an arbitrary number of harmonics can be suppressed. The system adapts itself and finds the right amplitudes and phases for all considered harmonics. The method needs some time to adjust all cancelling sine waves. Therefore, it is well suited for disturbances that stay constant over a period of time. This is given for the DC/DC converter considered in the following chapter.

IV. Demonstration

In this chapter, the algorithm of III is implemented on an FPGA system and applied to a DC/DC converter as Device Under Test (DUT). At first, the application and the test setup are explained. Afterward, the prototype system for the cancellation logic is introduced. The DUT is presented and details are given on the realization. The passive noise reduction of the deactivated cancellation system is investigated. Then, the active noise suppression for the complete frequency range of 150 kHz to 30 MHz is demonstrated. The power consumption of the cancellation system is estimated. At last, a frequency-selective variant of the method is presented.

A. Application

For demonstration, an evaluation board GS61008P-EVBHF is used as DC/DC converter that steps an input voltage of 48 V down to 12 V. The scheme of the buck converter is depicted in Figure 6. The switching frequency is set to 300 kHz. Since the duty cycle is kept constant, there are stable disturbing harmonics with a spacing of 300 kHz.

B. Test Setup

The test setup according to [1] is depicted in Figure 5. The overall setup is placed on a copper table as ground plane. The DUT consists of the DC/DC converter and the cancellation system that is presented in the following sections. The load for the 12 V output is a resistor with a resistance of 1 Ω. So, there is a transfer power of approximately 144 W. In reference to [1], an artificial network has been chosen for measurement of the conducted disturbances. The DUT is connected to the artificial network by one supply line above the measurement copper table. Therefore, only differential mode disturbances occur that are measured by an EMI receiver. A power supply provides the 48 V input voltage for the DUT via the artificial network.

For demonstration, the frequency range of 150 kHz to 30 MHz shall be suppressed actively in regard to the strictest limit (class 5) in [1] that comprises LW (150 kHz-300 kHz), MW (530 kHz-1.8 MHz), SW (5.9 MHz-6.2 MHz) and CB (26 MHz-28 MHz) radio. Due to the switching frequency of 300 kHz, there are 100 harmonics inside of the considered frequency range that must be suppressed. Peak and average emissions are mostly the same since the disturbances are stationary. Since the limit for the average emissions is much lower than for the peak emissions, the more critical average emissions are evaluated. According to [1], a resolution bandwidth of 9 kHz is used.

C. FPGA System

As a prototype platform for the cancelling logic, the FPGA system Red Pitaya STEMlab125-14 is used. It comprises a programmable FPGA, two DACs and two ADCs.

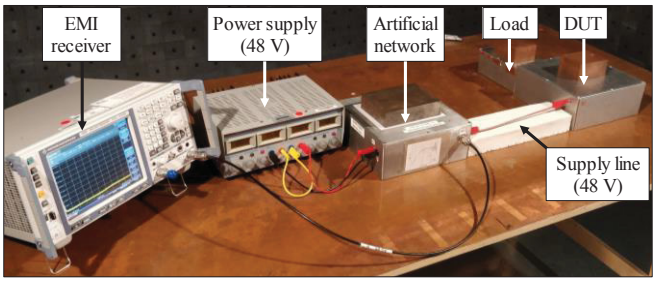

Figure 5: Photograph of the test setup

The ADCs and DACs exhibit a voltage range of ±1 V, a quantization of 14 bit, an analog bandwidth of 50 MHz and a sampling rate of 125 MS/s that is also used as a clock for the FPGA. The DAC is used for injecting the cancellation signals, and the ADC is used for sensing the resulting disturbances. For the given application, the limitations of the used hardware have been analyzed in [9]. The voltage range of ±1 V limits the measurable and producible signal. The quantization defines the signal-to-noise ratio (SNR) that is approximately 86 dB for 14 bit. From the voltage range and the SNR, the noise floor can be calculated to approximately 31 dBµV (rms value). This value correlates well with the residual disturbances after cancellation (note IV.F and IV.H). The suppressible frequency range is directly limited by the analog bandwidth of the ADCs and DACs. So, disturbances of up to 50 MHz can be suppressed.

Furthermore, the FPGA generates the control signal for the DC/DC converter. By doing so, there is a perfect synchronization between the disturbing and the cancelling system.

D. Device Under Test (DUT)

The schematics and a photograph of the realized DUT are depicted in Figure 6 or Figure 7, respectively. All parts are placed inside of a shielding enclosure that is also used as ground plane.

1) Sensor

For feedback measurement, a capacitive voltage sensor is applied to the 48 V supply line of the DUT. To avoid an overdrive of the FPGA system's ADC by harmonics of higher order, a low-pass filter with a cutoff frequency of 32 MHz has been applied. The ADC's dynamic range is well utilized, and there is no need for further adjustments.

2) Injector

As injecting circuit, an inductive transducer with a toroidal ferrite has been chosen. The primary and secondary windings consist of two turns each. Since there are only differential mode disturbances on the 48 V supply line, this differential mode injector is sufficient. To match the input impedance of the injector to the internal impedance of the FPGA system's DAC, an attenuator of 3 dB has been applied in series. There has been no need to further adjust the voltage range of the injector.

3) Auxiliaries

As stated before, the FPGA generates the control signal for the DC/DC converter. To avoid a ground loop over the control path and the sensing circuit that could degrade the precision of

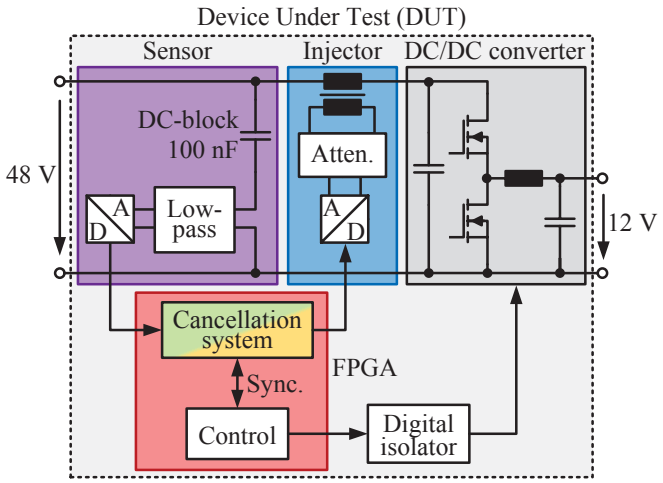

Figure 6: Schematic of the DUT

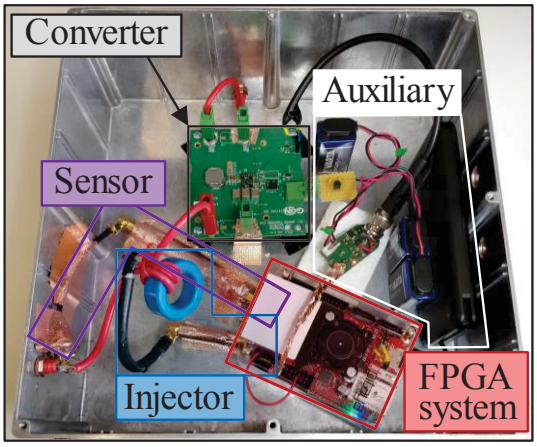

Figure 7: Photograph of the DUT

the feedback measurement, a digital isolator is applied. Additionally, there are a few auxiliary power supplies for the FPGA, for the power transistors' drivers and for the digital isolator.

E. Passive Attenuation of Cancellation System

By adding the sensor and the injector to the system, the disturbances are attenuated passively. To evaluate the influence, the disturbances are measured at the artificial network with and without the (still deactivated) cancellation system. The results are depicted in Figure 8. There is only a marginal noise reduction and the disturbances are still far above the class 5 limit. So, most of the noise suppression must be provided by the active cancellation.

F. Active Suppression of Cancellation System

In this section, the activated cancellation system is discussed and the results with and without active cancellation are shown in Figure 9. The disturbances are successfully suppressed for the complete frequency range of 150 kHz to 30 MHz. The fundamental wave is suppressed by approximately 60 dB and even the very high harmonics of up to 30 MHz are reduced by up to 40 dB. Now, the system's disturbances comply with the standard's class 5 limit [1]. It can be found that the residual disturbances tend to the noise floors of the ADCs and DACs of

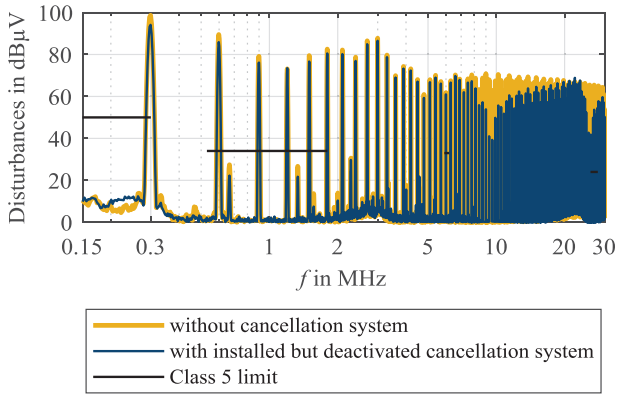

Figure 8: Disturbances without and with deactivated cancellation system

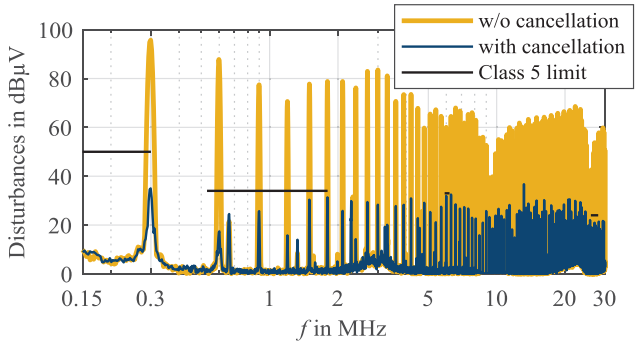

Figure 9: Disturbances without and with full cancellation

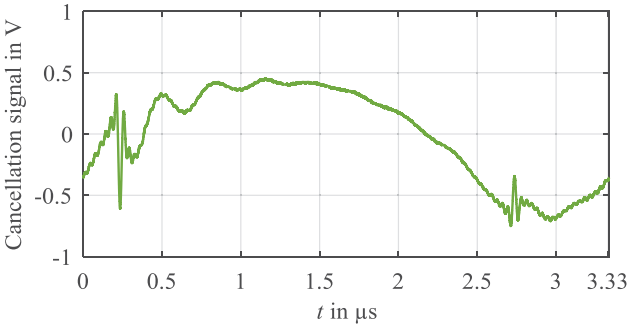

Figure 10: Successively adapted cancellation signal

31 dBµV. The successively adapted cancellation signal is measured by an oscilloscope and depicted in Figure 10.

G. Power Consumption of the Injector

To evaluate the power consumption of the injector, the rms value of the cancellation signal (Figure 10) is determined to $V_{\text{anti,rms}} \approx 384$ mV. Due to the 3 dB-attenuator, the DAC is terminated by $R_{\text{termination}} \approx 50\ \Omega$. The high frequency output impedance of the Red Pitaya STEMlab125-14 varies over frequency. For a worst-case approximation, the output impedance is assumed to be 0 Ω. Now, the power consumption of the FPGA can be estimated to 3 mW by (1). In comparison to the transfer power of 144 W, the injector losses are negligible.

$$P_{\text{anti}} = \frac{V_{\text{anti,rms}}^2}{R_{\text{DAC}} + R_{\text{termination}}} \quad (1)$$

H. Special Feature: Frequency Selective Cancellation

Considering the discontinuous limit line and the frequency-selective noise suppressing method presented in this work, it is also possible to eliminate only the harmonics that violate the class 5 limit. This special feature is demonstrated by the additional measurement in Figure 11. Here, the critical harmonics are suppressed below the standard's class 5 limit and the other harmonics remain untouched. The slight changes in the untouched harmonics are explained by harmonic distortion since the DAC and the analog circuitry are not ideally linear. Since the cancellation signal must only be optimized for 14 harmonics, the adaption process is significantly accelerated. Additionally, the power consumption of the injector is further reduced to approximately 2.8 mW.

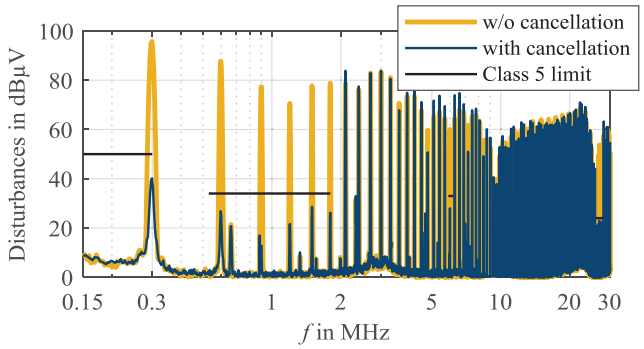

Figure 11: Frequency-selective cancellation of disturbances

V. Conclusion

In this work, a new method of successively constructing a synthesized cancellation signal has been developed and implemented on an FPGA system with fast Analog-to-Digital Converters and fast Digital-to-Analog Converters. In contrast to previous implementations, this method enables the successive suppression of an arbitrary number of harmonics by a stand-alone cancellation system. The cancellation system has been applied to the first 100 harmonics of a DC/DC converter in a wide frequency range of 150 kHz to 30 MHz. Previously, an external trainer and an arbitrary waveform generator were necessary to suppress such wide frequency ranges. The realization has been depicted, and the effectivity of the method has been proven by measurements. The investigations have shown the capability of successively adapted cancellation signals for wide-frequency application for the first time.

VI. Outlook

The cancellation system proves to be viable for disturbances that remain stationary over periods of time. Due to the necessary time for the successive adaption, the algorithm may not be applicable to frequently changing disturbances. To improve the applicability, the algorithm is currently being developed further to speed up the adaption process.

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