Active EMI Reduction of Stationary Clocked Systems by Adapted Harmonics Cancellation

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***Abstract*—Active cancellation of disturbing signals is a common method in EMC. In this paper, a specialized strategy is presented to minimize the disturbing harmonics of stationary clocked systems by injecting an appropriate harmonic cancellation signal with an adjustable signal synthesizer. The optimum cancellation signal is found via a convenient and robust adaptive approach. Each destructive harmonic is generated individually, and the cancelation signal is the superposition of a set of sinusoidal signals. As a special feature of this method, many troublesome effects, like delays or complex frequency characteristics, can be compensated easily. Several implementation variants can be derived from this general approach. Here, the variant, *continuously adapted harmonics cancellation* (CAHC), is considered. The system's limitations due to the ADC, the DAC, and the synchronization are described. An FPGA-implementation of CAHC is presented and applied to a dc/dc converter in an automotive component measurement setup to demonstrate the effectivity of the method.**

***Index Terms*—Adaptive, cancellation, clocked systems, EMI, harmonics.**

I. Introduction

CLOCKED systems, such as power electronic converters, tend to be considerable sources of EMI. To comply with international standards (e.g., [1] in automotive), the EMI is commonly reduced by the application of passive filters or shields that may be bulky, heavy, and expensive. Another strategy is the active cancellation of disturbing signals by a destructive interference between noise and antinoise [2]. This strategy is already commonly applied in EMC and acoustics, for example. In this work, an adaptive EMI cancellation strategy is developed for the application of stationary clocked systems. These systems comprise power electronics or digital systems working in one or more stationary operation modes. This work is built on [3] and [4].

For EMC, active EMI filters have been introduced in [5] and elaborated on in [6]–[8]. Like passive EMI filters, active filters are connected between the EMI source and sink. The disturbances are measured at the source and/or the sink, shaped by an analog circuit and injected back into the system in order to achieve a destructive interference between the signals. The possible structures of active filters are further generalized and analyzed in [9] and [10]. As power electronic converters steadily gain significance, there are, amongst many others, investigations on dc/dc converters, e.g., [11], motor inverters, e.g., [12], and PFC systems, e.g., [13]. Recently, comprehensive design guides have been developed for common mode [14], [15] and differential mode [16] active EMI filters. With the availability of very fast FPGAs and DSPs, more complex digital active EMI filters (DAEF) have been developed and investigated, e.g., switch mode power supplies [17], photovoltaic dc-to-ac microinverters [18], dc/dc converters [19], [20], and arc welding inverters [21]. For a perfect cancellation of the signals, noise and antinoise must be accurate opposites of each other and, therefore, exactly simultaneous. As the analog and/or digital signal processing of active filters causes an unavoidable delay, there are systematic limitations for the achievable reduction and the suppressible frequency range that are analytically described in this work. For stationary clocked systems, optimization potentials are identified to improve the effectiveness of active filters.

From these insights and with inspiration from the developments in active noise control (ANC) in acoustics [22], a specialized theory is derived for the EMI cancellation of stationary clocked systems: *harmonics cancellation* (HC). In this method, each harmonic is suppressed by an individual sine wave. The superposition of the sine waves results in a synthesized anti-EMI. To find the correct amplitudes and phases for compensation, HC is extended by an adaptive approach to *adapted harmonics cancellation* (AHC). From this theory, two implementation variants are formulated: 1) *continuously adapted harmonics cancellation* (CAHC) and 2) *previously adapted harmonics cancellation* (PAHC). For a digital realization, the systematic limitations of AHC are analyzed including the analog-to-digital converter (ADC), the digital-to-analog converter (DAC), and the synchronization to the clocked system. Then, CAHC is applied to a power electronic demonstrator in an automotive component measurement setup. To do so, a canceller is designed and an FPGA-implementation of narrowband ANC [23]–[25] is transferred to EMC. The effectivity of the method is proven by measurements with an artificial network and a rod antenna. A conclusion closes the work.

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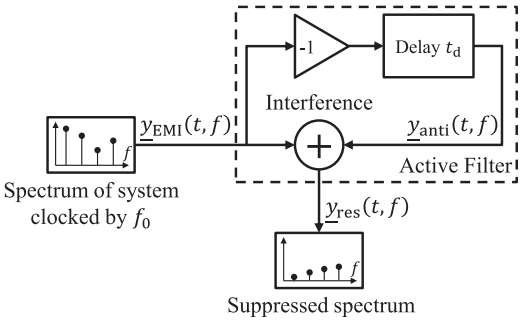

Fig. 1. Structure of feedforward active filters.

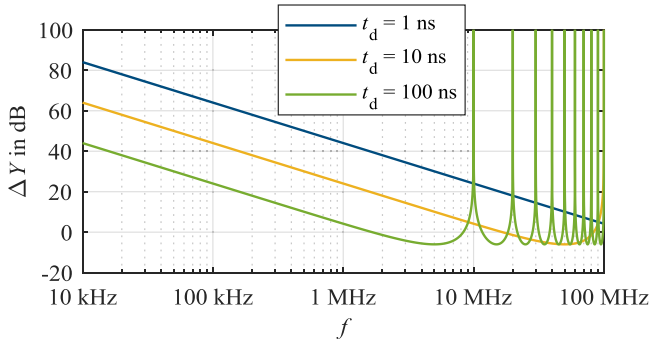

Fig. 2. Achievable reduction for different delay times.

II. Analysis of Active EMI Filters

Prior to introducing the proposed AHC, the current state of the art for EMI cancellation is discussed: active filters. The discussion includes the fundamental topologies, the influence of delay times on the achievable reduction, possible improvements for stationary clocked systems, and further potential for optimization.

A. Topologies

In general, there are feedforward and feedback active filters [9], [10]. In both strategies, the active filter is set between the EMI source and the EMI sink and reduces the disturbances at the sink. Feedback-types detect the disturbances directly at the sink and inject a compensation signal for suppression. Feedforward-types measure the disturbances at the EMI source and inject the inverted signal for cancellation. In theory, feedforward active filters nullify the disturbances completely if EMI and anti-EMI are the exact opposites of each other (phase-shift of 0° and inverted amplitude). In reality, due to, e.g., noise, the amplitudes cannot be exactly the same. Furthermore, all circuits contain delays due to factors like the slew rates of semiconductors or the finite propagation speed of electromagnetic signals. As feedforward-types theoretically offer infinite attenuations, they pose as a best case scenario for active filters. Since they are also easily mathematically described, feedforward-types are considered in the following investigation.

B. Influence of Delay Times

In this section, the impact of the unavoidable delay is analyzed. The assumed system is depicted in Fig. 1. The EMI source generates the stationary periodic disturbance $\underline{y}_{\mathrm{EMI}}(t,f)$ that propagates through the active filter. The feedforward active filter detects $\underline{y}_{\mathrm{EMI}}(t,f)$ and ideally inverts the signal by multiplying by -1. Due to the imperfections of real circuitry, this ideal signal is delayed by t_d and results in the anti-EMI $\underline{y}_{\mathrm{anti}}(t,f)$. EMI and anti-EMI are superposed to the residual disturbance $\underline{y}_{\mathrm{res}}(t,f)$.

Both EMI and anti-EMI can be described by the complex phasors (1) and (2) with $A \in \mathbb{R}^+$:

$$\underline{y}_{\mathrm{EMI}}(t,f) = A \cdot e^{j2\pi f \cdot t} \tag{1}$$

$$\underline{y}_{\mathrm{anti}}(t,f) = -A \cdot e^{j2\pi f \cdot (t-t_\mathrm{d})}. \tag{2}$$

The residual disturbance is calculated by the following:

$$\underline{y}_{\mathrm{res}}(t,f) = \underline{y}_{\mathrm{EMI}}(t,f) + \underline{y}_{\mathrm{anti}}(t,f). \tag{3}$$

To find the peak values of the disturbances, the absolute values are considered:

$$\left|\underline{y}_{\mathrm{EMI}}(t,f)\right| = A \tag{4}$$

$$\left|\underline{y}_{\mathrm{res}}(t,f)\right| = A \cdot \sqrt{2 - 2\cos(2\pi f \cdot t_\mathrm{d})}. \tag{5}$$

To find the achievable reduction $\Delta Y(f)$, the quotient of the peak values is investigated:

$$\Delta Y(f) = 20\ \mathrm{dB} \cdot \log_{10}\left(\frac{\left|\underline{y}_{\mathrm{EMI}}(t,f)\right|}{\left|\underline{y}_{\mathrm{res}}(t,f)\right|}\right). \tag{6}$$

Inserting (4) and (5) into (6) results in the following:

$$\Delta Y(f) = -10\ \mathrm{dB}\log_{10}\left(2 - 2\cos(2\pi f \cdot t_\mathrm{d})\right). \tag{7}$$

Exemplary, for delay times of 1, 10, and 100 ns, the achievable reductions are depicted in Fig. 2. Shorter delay times result in higher reductions as the anti-EMI is better synchronized with the EMI. For higher spectral frequencies, the same delay time causes a more severe phase-shift. Therefore, EMI and anti-EMI drift apart and the achievable reduction drops. So, the circuitry delay is a limiting factor for the achievable reduction and the suppressible frequency range. For spectral frequencies of $f = m/t_\mathrm{d}$ with $m \in \mathbb{N}$, infinite reductions follow from (7). In these cases, the delay time causes a phase-shift of $m \cdot 360°$ for the respective spectral frequency. So, for stationary signals, there is ideally a perfect cancellation.

C. Improvements for Stationary Clocked Systems

Under the assumption of a stationary clocked system with a fundamental frequency of f_0, there is generally a disturbing spectrum according to (8). The factor 2 is introduced to describe the one-sided spectrum [26].

$$\underline{Y}_{\mathrm{clocked}}(f) = \sum_{k=1}^{K} 2\left|c_\mathrm{k}\right| e^{j\angle c_\mathrm{k}} \cdot \delta(f - kf_0). \tag{8}$$

The spectrum consists of K harmonics with a spacing of f_0 that must be cancelled out. By applying an additional and

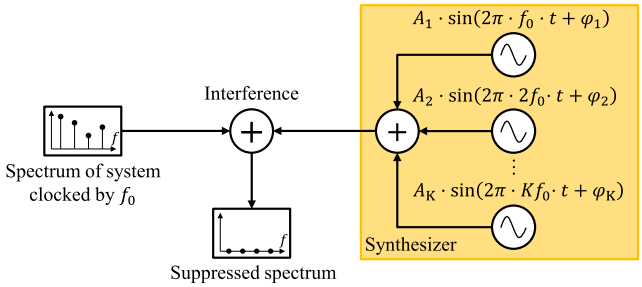

Fig. 3. Principle of HC.

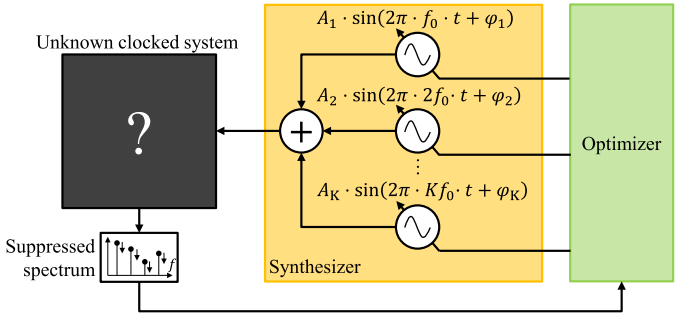

Fig. 4. Principle of AHC.

artificial delay t_{add}, the frequency points with infinite reductions of (7) may be shifted onto the disturbing harmonics:

$$m/\left(t_{\mathrm{d}} + t_{\mathrm{add}}\right) = kf_0. \tag{9}$$

For the fundamental wave $(k = 1)$, a phase-shift of 360° $(m = 1)$ is chosen. Hence, an additional delay of $t_{\mathrm{add}} = 1/f_0 - t_{\mathrm{d}}$ results from (9). For the higher harmonics $(k > 1)$, $m = k$ follows from (9). So, for the kth harmonic, there is a phase-shift of $k \cdot 360°$ in the cancellation signal. Therefore, in theory, all harmonics are infinitely suppressed. As a more intuitive explanation, the additional delay causes a total delay time of one clock period. Due to the stationarity of the disturbances, the signal of the prior period also fits to the later period. Therefore, the delay time of the circuitry is successfully compensated, and the effectivity of the method is widely improved.

D. Optimization Potentials

For high orders k of the harmonics, very large phase-shifts of $k \cdot 360°$ result. So, small deviations in the determined additional delay time t_{add} can cause severe phase errors for high frequencies. Furthermore, especially for high frequencies, there are additional phase and magnitude responses due to the active filter's circuit that must be compensated as well. As these are not considered yet, complex transfer functions must be implemented for compensation. To resolve these issues, HC and AHC are introduced in the following.

III. Novel Strategies for Active EMI Cancellation

In this chapter, a novel strategy is derived for active cancellation of switching harmonics. For the application of a stationary clocked system, HC is motivated and introduced. To easily and precisely find the necessary cancelling parameters for complex or even unknown systems, the method is extended by an adaptive approach to AHC. Afterward, a general realization of a digital AHC with its sensor and injector is presented. Then, two elemental realization variants are briefly introduced: 1) CAHC and 2) PAHC.

A. Harmonics Cancellation

Clocked systems, like power electronic converters in a stationary state, cause distinctive harmonics with a spacing of the fundamental frequency f_0. To suppress the disturbances of such a system in a specific frequency range, only the harmonics must be eliminated. This is the basic idea of HC as depicted in Fig. 3. By applying HC, the first $K \in \mathbb{N}$ disturbing harmonics will be cancelled out. For each harmonic $k \leq K$, a synthesizer generates a corresponding sine wave with such an amplitude A_{k} and such a phase φ_{k} that there is a destructive interference for the specific frequency.

B. Adapted Harmonics Cancellation

In reality, there are often complex systems that are very difficult to characterize (especially for high frequencies). For a simple and effective parametrization of the sine waves, AHC (see Fig. 4) is introduced. In general, there is the presented synthesizer of anti-EMI and an unknown clocked system with a switching frequency of f_0. The interference between the EMI and the anti-EMI causes a resulting spectrum that will be reduced. To do so, an optimizer sets the amplitudes A_{k} and phases φ_{k} of the sine waves in such a way that the feedback signal is minimized. By this method, each sine wave is optimized independently in its respective amplitude A_{k} and phase φ_{k}. So, there is no need to characterize or construct complex transfer functions for a successful cancellation. Additionally, there are basically no limitations for the system's structure; by the simple parametrization of the sine waves, all bothersome unknown effects, like delays, phase-shifts or attenuations, can be compensated and, therefore, neutralized.

C. Digital AHC

To apply AHC to a clocked system, a sensor for disturbance measurement and an injector for the input of the cancellation signal are necessary to connect the canceller to the clocked system. The basic structure is depicted in Fig. 5. Again, there is the clocked system, the optimizer, and the synthesizer for the cancellation signal. To find the feedback signal, the spectrum is measured by a sensor. This sensor consists of a sensing circuit and an ADC for the digitization of the signal. The sensing circuit may be realized by, e.g., a decoupling capacitor or an antenna. The ADC may be realized with an integrated circuit or even with an EMI receiver. The cancellation signal is brought into the clocked system by an injector that consists of a DAC and, e.g., an inductive transducer as the injecting circuit. As the cancellation signal is adapted to the whole system, there are basically no restrictions for the structure of the injectors, sensors or clocked systems. To synchronize the cancellation signal

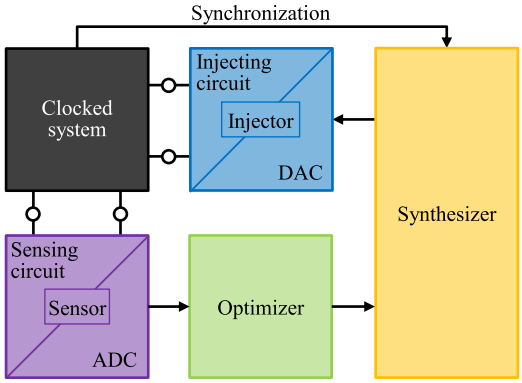

Fig. 5. Structure of digital AHC.

to the disturbances, the synthesizer is directly triggered by the clocked system. This trigger must be correlated to the disturbances and not eliminated by the cancellation. Control signals are especially convenient as they are highly correlated to the disturbances, can be measured easily, and are not influenced by the cancellation.

D. Implementation Variants of Digital AHC

There are many possible implementation variants to apply AHC to a clocked system. At this point, two elemental strategies are introduced: 1) CAHC and 2) PAHC. In CAHC, the total structure of Fig. 5 is implemented inside of the device. So, there is a continuous adaption to the disturbances compensating all changes of the system with some delay due to the optimization algorithm. As the disturbances are rather deterministic, it is also possible to use an external trainer to teach-in the canceller. This is the basic idea of PAHC where the sensor, optimizer, and parts of the synthesizer are outsourced into an external trainer. The teach-in process of the canceller can be done previously during development, after manufacturing, after installation or during maintenance.

E. Comparison to Analog and DAEF

In comparison to analog and/or digital active filters, HC employs a completely different approach for the generation of the anti-EMI. Feedforward active filters measure the disturbances at the source and inject this signal weighted by a transfer function back into the system. Feedback active filters measure the disturbances at the sink, apply this signal to an appropriate transfer function and inject it back into the system. So, for both feedforward- and feedback-types, the anti-EMI is generated from the measured disturbance signal. In AHC, the anti-EMI is artificially synthesized inside of the digital system. Therefore, the feedback-loop of AHC is only required for correction of the synthesized compensation signal.

For active filters, there are some restrictions for the feasible topologies. In feedforward-types, the anti-EMI must be a precise opposite of the measured EMI. So, simple topologies (current-sensing current-injecting or voltage-sensing voltage-injecting) are preferred as they only need a transfer function of ideally -1. Other topologies suffer from load dependencies and/or complex transfer functions that must be compensated. For feedback-types, voltage- and current-sensing and voltage- and current-injecting can be combined freely. Nevertheless, due to stability reasons, there are some restrictions. Due to the adaptive approach of AHC, there is basically no limitation for the systems structure. As an example, an E-field sensing and an inductive voltage injection can be combined.

Of course, the hardware expenses for analog active filters can be lower than for AHC. Nevertheless, the achievable attenuation and the suppressible frequency range of analog active filters are systematically limited by intrinsic delay times. Due to the synthesis method and the adaptive approach, the limitations of active filters do not apply for AHC. As FPGAs and DSPs are integrated into an increasing number of devices and maybe only a small portion of the digital system's capacity is needed for the cancellation algorithm, cost-efficient solutions are possible.

This basic idea has also been realized in DAEF [17]–[21]. In this strategy, the FPGA controls the power electronic system and also generates the anti-EMI. Comparable to analog active EMI filters, DAEFs shape a measured signal to generate the anti-EMI. In this method, the FPGA's capabilities are used for an advanced signal processing. As discussed in [21], the delay times are a limiting factor not only for analog active EMI filters but for digital implementations as well. Possible solutions for stationary systems are mentioned in [21] and realized in [20]. In AHC, the FPGA's capabilities are utilized for a simple adaptive approach that requires only little signal processing. Since sine waves are generated in AHC, delay times can easily be compensated by phase-shifts.

IV. Systematic Limitations of Digital AHC

In this chapter, the systematic limitations of a digitally implemented AHC are analytically derived that apply to both CAHC and PAHC. The most important measures include the resolution of the ADC and the DAC and the synchronization of the synthesizer.

A. Limitations Due to the ADC's Resolution

The ADC is a central component as it closes the feedback loop to the optimizer. For the digitalization of the sensed signal, various concepts can be realized. In this chapter, a high-speed ADC is considered in more detail. Further sensor concepts are briefly introduced.

1) High-Speed ADC: At first, a high-speed ADC with a sampling rate much higher than the fundamental frequency of the clocked system is considered. So, there is a digitized time signal with a frequency range from dc to half of the sampling rate due to the Nyquist–Shannon sampling theorem. AHC can only be applied to this frequency range as higher frequencies cannot be measured [4]. With AHC, the harmonics are adaptively suppressed. As shown in [4], the adaption stops if the error signal falls under the noise level $V_{\mathrm{ADC,NF}}$ of the ADC. So, under the consideration of a constant transfer function of 1 for the sensing circuit, all harmonics are suppressed to the same residual disturbance level $V_{\mathrm{ADC,NF}}$. These limitations are illustrated in Fig. 6.

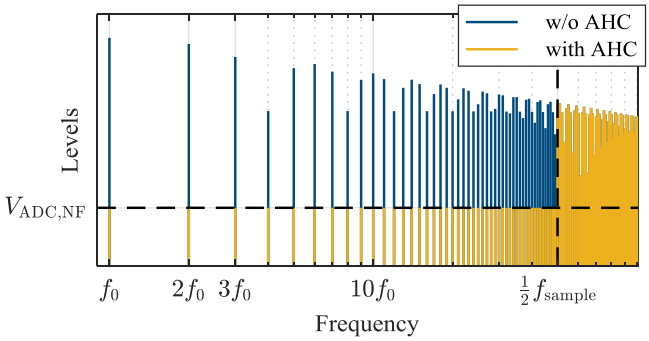

Fig. 6. ADC limits for AHC.

The ADC can be characterized by two important measures: The maximum measurable voltage $V_{\mathrm{ADC,max}}$ and the number of bits b_{ADC}. Since an overdrive of the ADC would corrupt the measurement, the voltage of the measurement signal must be below $V_{\mathrm{ADC,max}}$ at all points in time. If the measurement signal is much higher than $V_{\mathrm{ADC,max}}$, the total level must be reduced by, e.g., a broadband attenuator or a filtering of unconsidered frequency ranges. If the measurement signal is far below the maximum measurable voltage, the dynamic of the ADC is poorly utilized. In this case, the signal should be increased by changing the sensing circuit or the amplifier.

As previously explained, the harmonics are adaptively reduced until they drop below the noise floor. To describe this level, the signal-to-noise ratio (SNR) is considered defining the quotient of the highest measurable sine wave ($V_{\mathrm{ADC,max}} - 3$ dB) and the noise floor (both in RMS values) in dependence of b_{ADC}:

$$\Delta V_{\mathrm{ADC,SNR}} = b_{\mathrm{ADC}} \cdot 6.02\ \mathrm{dB} + 1.76\ \mathrm{dB}. \tag{10}$$

The noise floor can be calculated by

$$V_{\mathrm{ADC,NF}} = V_{\mathrm{ADC,\,max}} - 3\ \mathrm{dB} - \Delta V_{\mathrm{ADC,SNR}}. \tag{11}$$

In practical applications, there is usually a limit that must be fulfilled (e.g., [1]) in a specific measurement setup. Under consideration of the transfer functions between the standard's noise sink (e.g., artificial network or current probe) and the sensor's ADC, the standard's limit can be transferred to the limit $V_{\mathrm{ADC,limit}}$ measured by the ADC. As all harmonics are basically suppressed to the noise floor $V_{\mathrm{ADC,NF}}$, it must be set below $V_{\mathrm{ADC,limit}}$ to comply with the limit of the standard:

$$V_{\mathrm{ADC,NF}} \leq V_{\mathrm{ADC,limit}}. \tag{12}$$

So, the necessary number of bits b_{ADC} can be derived from (10)–(12):

$$b_{\mathrm{ADC}} \geq \frac{V_{\mathrm{ADC,max}} - V_{\mathrm{ADC,limit}} - 4.76\ \mathrm{dB}}{6.02\ \mathrm{dB}}. \tag{13}$$

2) EMI Receiver: As stated in Section III-C, it is also possible to utilize an EMI receiver as an ADC. Especially for PAHC, an EMI receiver is an excellent choice as it offers a very high dynamic and, therefore, a very high SNR.

3) Bandpass, Detector, and Slow ADC: To find a cheaper implementation for CAHC, a concept similar to an EMI receiver may be realized with simple hardware. The considered harmonic can be isolated by a bandpass-filter and evaluated by a peak detector. Now, there is basically a constant value that can be measured by a slow ADC. In comparison to the high-speed ADC, the hardware requirements are widely reduced. Since there is only one harmonic measured at each point in time, the whole SNR of the ADC can be utilized as it describes the quotient of the highest measurable sine wave and the noise floor. On the downside, the optimizer cannot simultaneously adapt the cancellation signal for multiple harmonics. Therefore, the cancellation signal must be successively constructed from harmonic to harmonic.

4) Broadband Power Meter and Slow ADC: Furthermore, it is possible to evaluate the total RMS value of a specific frequency range. In respect to each harmonic, there is a cancellation signal that minimizes the total power of the disturbances. So, by sequential adjustment of the cancellation signal for each harmonic, a wide spectrum can be suppressed. Again, the ADC may be slow but very precise.

B. Limitations Due to the DAC's Resolution

The injector of the canceller utilizes a DAC to generate the compensation signal for the disturbed system. The required sample rate is defined by doubling the highest frequency of the compensation signal due to the sampling theorem. Nevertheless, higher sample rates are recommended to reduce bothersome effects such as aliasing.

Due to analogy, the considerations of the sensor's ADC can be transferred to the injector's DAC. Again, the maximum voltage of the cancellation signal must be brought close to $V_{\mathrm{DAC,max}}$ to utilize most of the DAC's SNR. If a small signal is necessary, the output signal of the DAC may be reduced by, e.g., an attenuator. If a large signal is required, the output signal of the DAC may be increased by changing the injecting circuit or the amplifier. The necessary number of bits b_{DAC} may be calculated by the same formula as (13):

$$b_{\mathrm{DAC}} \geq \frac{V_{\mathrm{DAC,max}} - V_{\mathrm{DAC,limit}} - 4.76\ \mathrm{dB}}{6.02\ \mathrm{dB}}. \tag{14}$$

For an optimized system design, both ADC and DAC should have the same number of bits $b_{\mathrm{ADC}} = b_{\mathrm{DAC}}$ to avoid mutual limitation of the converters.

C. Synthesizer

For the synthesizer, there are basically two aspects that limit the effectivity of AHC. The first is the quantization of the synthesized signal. Of course, the injector and the synthesizer should not limit each other. So, in an optimized system design, the injector's DAC and the synthesizer should have the same number of bits $b_{\mathrm{DAC}} = b_{\mathrm{synth}}$. The second aspect is the jitter that may occur when triggering the canceller. In the following, this effect is analyzed in detail.

1) Jitter of Synchronization Signal: The first source of jitter may be the external trigger signal, itself. So, a signal must be chosen that is as stable as possible. In, e.g., power electronics, there are control signals for the power transistors that are very

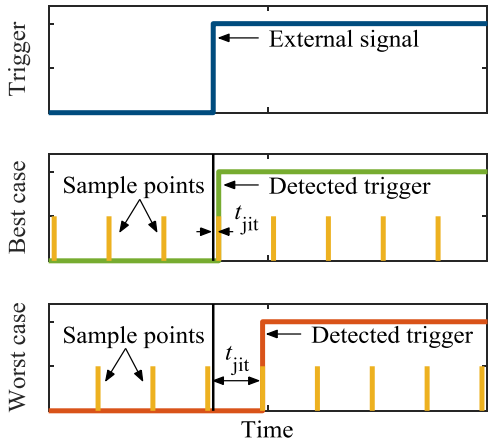

Fig. 7. Jitter due to trigger detection.

stable, digitally available, and also highly correlated with the disturbances. With such a signal, the trigger's jitter may be negligible. In the following, an ideal trigger signal without any jitter is assumed.

2) Jitter Due to Trigger Detection: Now, the jitter-free trigger signal must be detected by the canceller. As a digital canceller is considered, the system checks for a change in the trigger signal at every discrete sample point (see Fig. 7).

In the best case, the system samples right after the external trigger signal, and there is basically no trigger delay. In the worst case, the system samples right before the external trigger signal, so, the canceller detects the trigger signal one sample period later. In the end, the possible jitter error is uniformly distributed in the interval $[0, T_{\mathrm{sample}})$.

3) Effect on the Cancellation: Due to the jittering, EMI $\underline{y}_{\mathrm{EMI}}(t,f)$ and anti-EMI $\underline{y}_{\mathrm{anti}}(t,f)$ drift apart, and the effectivity of the cancellation drops. By substituting t_{d} with t_{jit}, (7) can be applied again:

$$\Delta Y(f) = -10\ \mathrm{dB} \log_{10}\left(2 - 2\cos\left(2\pi f \cdot t_{\mathrm{jit}}\right)\right). \tag{15}$$

As t_{jit} varies for each trigger in the interval of $[0, T_{\mathrm{sample}})$, there is a differing momentary reduction $\Delta Y(f)$ for each trigger period. In the following, its effect on the suppression of the peak and average emissions is analyzed.

a) Suppression of peak emissions: The peak emissions are determined by the highest disturbance that appears for a specific frequency. Therefore, the minimally occurring reduction is dominant:

$$\Delta Y_{\mathrm{PK}}(f) = \min\left\{-10\ \mathrm{dB} \log_{10}\left(2 - 2\cos\left(2\pi f \cdot t_{\mathrm{jit}}\right)\right)\right\}. \tag{16}$$

For $t_{\mathrm{jit}} \in [0, T_{\mathrm{sample}})$, the minimum can be described as

$$\text{for } f < \frac{1}{2 \cdot T_{\mathrm{sample}}}:$$

$$\Delta Y_{\mathrm{PK}}(f) = -10\ \mathrm{dB} \log_{10}\left(2 - 2\cos\left(2\pi f \cdot T_{\mathrm{sample}}\right)\right) \tag{17}$$

$$\text{for } f \geq \frac{1}{2 \cdot T_{\mathrm{sample}}}: \Delta Y_{\mathrm{PK}}(f) = -6\ \mathrm{dB}. \tag{18}$$

It is also worth mentioning, for spectral frequencies of $1/(2 \cdot T_{\mathrm{sample}})$ and higher, the peak disturbances are increased by 6 dB due to the possible jitter error.

b) Suppression of average emissions: For the average emissions, the relationship between the RMS values must be considered:

$$\Delta Y_{\mathrm{AVG}}(f) = 20\ \mathrm{dB} \cdot \log_{10}\left(\frac{\mathrm{RMS}\left(\left|\underline{y}_{\mathrm{EMI}}\right|\right)}{\mathrm{RMS}\left(\left|\underline{y}_{\mathrm{res}}\right|\right)}\right). \tag{19}$$

In analogy to (4) and (5), the following description results:

$$\left|\underline{y}_{\mathrm{EMI}}(t,f)\right| = A \tag{20}$$

$$\left|\underline{y}_{\mathrm{res}}(t,f)\right| = A \cdot \sqrt{2 - 2\cos\left(2\pi f \cdot t_{\mathrm{jit}}\right)}. \tag{21}$$

The RMS values must be calculated for $t_{\mathrm{jit}} \in [0, T_{\mathrm{sample}})$ by

$$\mathrm{RMS}(y) = \sqrt{\frac{1}{T_{\mathrm{sample}}} \cdot \int_0^{T_{\mathrm{sample}}} y^2 \, dt_{\mathrm{jit}}}. \tag{22}$$

Combining and transforming (19)–(22) results in

$$\Delta Y_{\mathrm{AVG}}(f) = -10\ \mathrm{dB} \cdot \log_{10}\left(2 - 2\,\mathrm{sinc}\left(2\,T_{\mathrm{sample}}\,f\right)\right). \tag{23}$$

4) Limitation of the Canceller: As analyzed, the jitter error causes a limitation for the achievable reduction of both the average and peak emissions. So, in order to fully utilize the capabilities of the overall canceller (including the sensor's ADC and the injector's DAC), the synchronization of the synthesizer must be given special attention. The canceller and the clocked system control may be implemented on the same hardware to nullify the trigger error. By this measure, there is an intrinsic synchronicity ($t_{\mathrm{jit}} = 0$) resulting in an unlimited attenuation ($\Delta Y_{\mathrm{PK}}(f) \to \infty$ dB and $\Delta Y_{\mathrm{AVG}}(f) \to \infty$ dB), theoretically. In this case, the ADC and the DAC determine the achievable reduction again.

V. Application Example of CAHC

In this chapter, the method CAHC is applied to a demonstrator setup. First, the test setup is introduced. Then, a possible implementation for CAHC is presented and realized in an FPGA-system. Afterward, the effectiveness of the method is shown by measurements.

A. Test Setup

For demonstration purposes, CAHC is applied to a dc/dc converter. The test setup is depicted in Figs. 8 and 9, and it is described in more detail below. For sensing and injecting, a voltage-sensing voltage-compensation topology has been chosen. Due to the adaptive approach, other topologies can be utilized as well.

1) Clocked System: As clocked system, the evaluation board GS61008P-EVBBK is considered. This dc/dc converter steps down the input voltage of 48 V to 12 V for a resistive load of 1 Ω. The converter is operated with a switching frequency f_0 of 300 kHz and a constant duty cycle of approximately 25%.

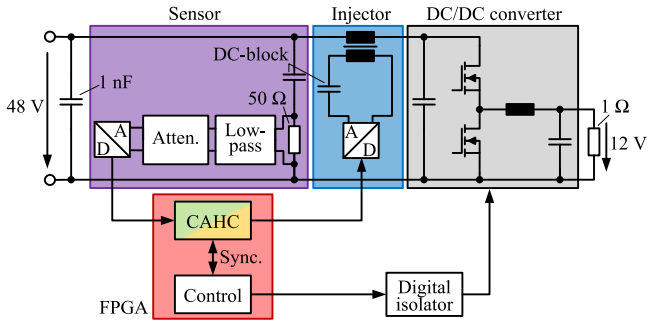

Fig. 8. Schematics of the test setup.

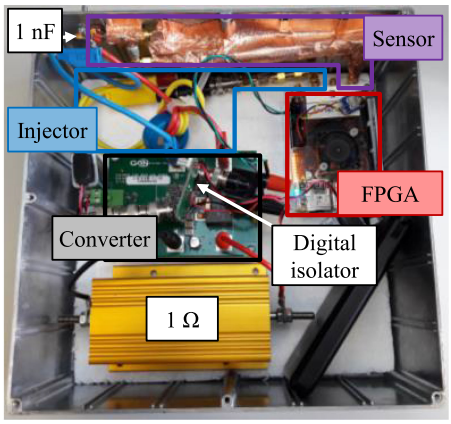

Fig. 9. Photograph of the test setup.

For demonstration purposes, the average disturbances of the primary side (48 V) will be suppressed in respect to class 5 in the frequency range of 150 kHz–1.8 MHz (LW and MW [1]). To comply with this class, the conducted disturbances at the input of the system must be suppressed below 34 dBµV for frequencies over 530 kHz.

2) FPGA-System: As a prototype for the cancelling logic, an FPGA-system with two DACs and two ADCs, Red Pitaya STEMlab 125-14, is used. The system's ADCs and DACs exhibit a voltage range of ± 1 V at 50 Ω, a quantization of 14 bit, a bandwidth of 50 MHz and a sampling rate of 125 MS/s that is also used as a clock for the FPGA. From (10) and (11), there is a noise floor of 31 dBµV as a result of the DACs and ADCs. CAHC is implemented on the FPGA, itself. From Section IV-C, it can be found that external triggering would limit the achievable reduction due to a possible jitter error. To eliminate the jitter and gain a full synchronicity between the systems, the dc/dc converter is controlled by the FPGA, itself.

3) Sensing Circuit: The disturbances are measured over a resistor of 50 Ω. To block the nominal voltage of 48 V, a dc-block capacitor of 100 nF is applied in series. To avoid an overdrive of the FPGA-system's ADC (note Section IV-A.1), a low-pass filter with a cutoff frequency of 2.5 MHz is applied. To suppress resonances between the low-pass filter and the overall system, a 3 dB attenuator is connected in series. This value is measured by the ADC and passed to the FPGA. Under the assumption of a transfer function of 1 for the sensing circuit in the considered frequency range, the noise floor of 31 dBµV is below the limit of the standard.

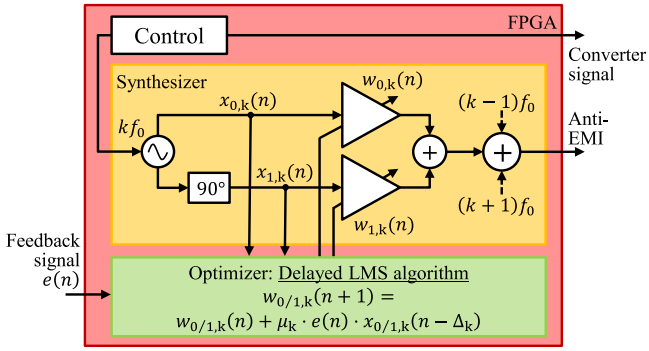

Fig. 10. Implementation of CAHC.

4) Injecting Circuit: An inductive transducer with a toroidal ferrite is chosen as the injecting circuit. The primary and secondary windings consist of two turns each. So, ideally, there is a transformation ratio of 1. To block a possible dc-offset of the FPGA-system's DAC, a capacitor of 100 nF is connected in series. A magnitude response from DAC to ADC of approximately -6 dB has been found by measurement for the considered frequency range. So, the DAC must inject double the voltage that is measured by the ADC. As the DAC is still not overdriven and the noise floor of 31 dBµV is much lower than the required precision of 34 dBµV + 6 dB = 40 dBµV, the voltage range of the DAC is not adjusted any further.

5) Further Details: To avoid a ground loop that may corrupt the measurement of the FPGA-system's ADC, a digital isolator is utilized for the control signal of the dc/dc converter.

As stated beforehand, the harmonics in the frequency range of 150 kHz–1.8 MHz are considered. So, higher harmonics are not suppressed by CAHC. To avoid an overdrive of, e.g., the broadband antenna amplifier, the higher frequencies are attenuated by a capacitor of 1 nF at the output of the device. Since this value is rather low, there is no significant influence on the first harmonics of the system.

The test system is placed in a closable aluminum case so that only the supply line is measured in the antenna measurement.

B. FPGA-Implementation

Fig. 10 schematically depicts one possible implementation of CAHC. The canceller is based on [24] and [25] and implemented on the programmable FPGA-system. The logic is known under the name of "single-frequency adaptive notch filter" and is well established in the ANC of acoustical phenomena [22]. Note that this structure can also be used to initially find the cancellation signals or parameters for PAHC.

In this implementation, an arbitrary sine wave $x_{0,\mathrm{k}}(n)$ with the frequency kf_0 is generated. This sine wave is triggered by the same signal that also controls the clocked system. To adjust the sine wave's amplitude A_k and phase φ_k, an orthogonal system is created by a phase-shift of 90° of the generated sine wave. Both the original $x_{0,\mathrm{k}}(n)$ and the phase-shifted signal $x_{1,\mathrm{k}}(n)$ are respectively multiplied by the factors $w_{0,\mathrm{k}}(n)$ and $w_{1,\mathrm{k}}(n)$

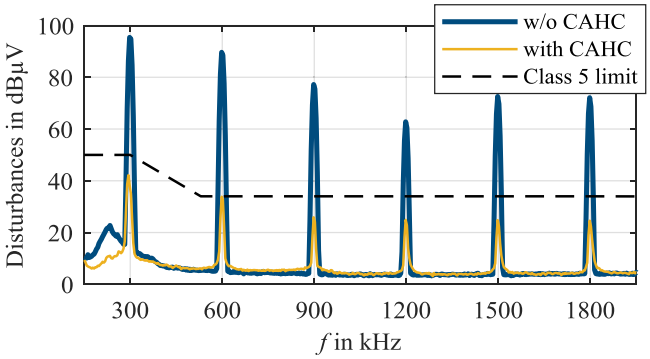

Fig. 11. Artificial network measurement.

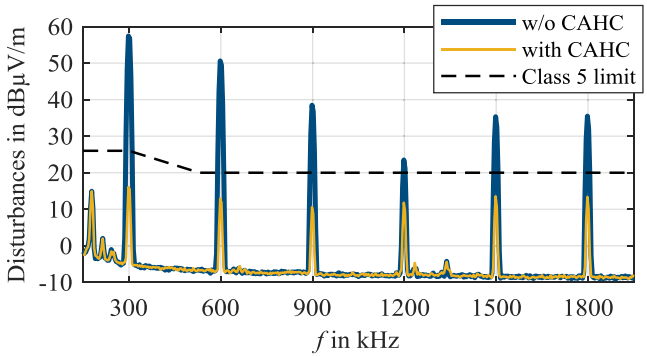

Fig. 12. Rod antenna measurement.

and summated. Any sine wave with the frequency kf_0 can be created by adjusting these factors.

To find the optimum sine wave, the factors $w_{0,\mathrm{k}}(n)$ and $w_{1,\mathrm{k}}(n)$ are derived from the delayed LMS algorithm [27], [28]. This algorithm basically compares the error signal $e(n)$ with the generated signals $x_{0/1,\mathrm{k}}(n)$ and adjusts the factors $w_{0/1,\mathrm{k}}(n)$ to minimize the error. Note that the algorithm intrinsically optimizes only the harmonic that corresponds to the generated sine wave. So, an additional frequency selection, like filtering or FFTs, is not necessary for the error signal. For the stability of the algorithm, it is crucial that the signals are correlated in time. As DACs, ADCs, and analog circuitries cause delays in the propagation of the signals, $e(n)$ is measured much later than $x_{0/1,\mathrm{k}}(n)$ is generated. Therefore, the total delay Δ_k of the path from injecting to sensing is respected in the update rule of the algorithm. The remaining variable μ_k is the step size of the algorithm. A large μ_k speeds up the convergence of the algorithm but may cause instability [29]. As there is a stationary operation of the system in this work, a very small μ_k is chosen for a precise adaption [30], [31].

To suppress multiple harmonics, one solution is to parallelize the depicted structure and to superpose the output signals [22]. In Fig. 10, the synthesized sine waves for the harmonics $k-1$, k, and $k+1$ are summated. The presented structure is implemented on the FPGA-system for each of the six disturbing harmonics in the considered frequency range. Of course, the FPGA-system must have sufficient resources to optimize and generate the required number of sinusoidal signals. In order to save resources, a sequential approach is proposed. In this approach, the structure of the single-frequency adaptive notch filter is sequentially applied to one harmonic after the other, starting from the lowest frequency. The determined cancellation signals are superposed to successively construct the total cancellation signal. Theoretically, an arbitrary number of harmonics can be suppressed by this strategy.

C. Measurement With Artificial Network

Fig. 11 illustrates the average measurements at the artificial network with and without active CAHC. The test setup is set according to [1]. As required, the first six harmonics are suppressed by 53, 56, 51, 38, 48, and 48 dB, respectively, and they comply with the class 5 limit. In conformity with the theory, higher harmonics are not significantly influenced.

D. Measurement With Rod Antenna

In Fig. 12, the average measurements for a rod antenna are depicted. Again, the measurement is done according to [1]. By applying CAHC, the disturbances are suppressed below the given limit.

VI. Conclusion

In this work, a specialized theory for cancelling the EMI of stationary clocked systems has been introduced: AHC. From this theory, and for a digital realization, the implementation variants CAHC and PAHC have been derived. The systematic limitations of the sensor's ADC, the injector's DAC, and the synchronization have been studied analytically. For demonstration purposes, CAHC has been implemented on an FPGA-system with fast and accurate ADCs and DACs. The cancellation system has been applied to a dc/dc converter in an automotive component measurement setup in the frequency range of 150 kHz–1.8 MHz. Due to the suppression of up to 56 dB, the converter complies with the class 5 limit. Since only the bandwidth of the cancellation system limits the suppressible frequency range and the utilized FPGA-system has a bandwidth of 50 MHz, the technological limits are not reached in the investigations presented here. All in all, AHC proves to be a very efficient method for suppressing the disturbances of stationary clocked systems.

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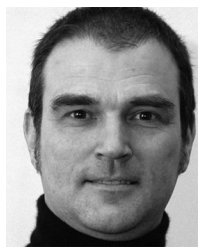

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