

Development of an Adaptive EMI Cancellation Strategy for Stationary Clocked Systems

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Abstract—Cancellation of disturbing signals is a common strategy in EMC. In this work, a specialized strategy is developed to cancel the disturbing harmonics of stationary clocked systems. This strategy is refined by an adaptive approach to conveniently find the optimum signals for cancellation. As a special feature of this method, all troublesome effects, like delays or attenuations, can easily be compensated. From a basic theory, two implementation variants are derived: 1) *Continuously Adapted Harmonics Cancellation (CAHC)* and 2) *Previously Adapted Harmonics Cancellation (PAHC)*. CAHC is implemented on an FPGA-system. The hardware, programming and performance of the utilized FPGA and its peripherals are transparently discussed. The effectivity of the method is demonstrated for a power electronic dc-to-dc converter.

Keywords—*Adaptive; Cancellation; Clocked Systems; EMI; FPGA; Harmonics*

I. INTRODUCTION

Clocked systems like power electronic converters tend to be considerable sources of EMI. To comply with international standards (e.g. [1] in automotive), the EMI is commonly reduced by the application of passive filters or shields that may be bulky, heavy and expensive. Another strategy is the active cancellation of disturbing signals by a destructive interference between noise and anti-noise [2]. This strategy is already commonly applied in, e.g., EMC and acoustics. In this work, an adaptive EMI cancellation strategy is developed for the application of stationary clocked systems. These systems comprise, e.g., power electronic converters in steady operating points.

For EMC, active EMI filters are well known. Like passive EMI filters, active filters are connected in between the EMI source and sink. The disturbances are measured at the source and/or the sink, shaped by an analog circuit and injected back into the system to achieve a destructive interference between the signals. For active filters, there are some fundamental topologies that are generalized and analyzed in [3] and [4]. For a perfect cancellation of the signals, noise and anti-noise must be accurate opposites of each other and, therefore, exactly simultaneous. As the analog and/or digital signal processing of active filters causes an unavoidable delay, there are systematic limitations for the achievable reduction and the suppressible frequency range that are analytically described in this work.

From these insights and inspired by the developments in Active Noise Control (ANC) in acoustics [5], a specialized theory is derived for the EMI cancellation of stationary clocked systems: *Harmonics Cancellation (HC)*. To find the parameters for

compensation, this method is extended by an adaptive approach to *Adapted Harmonics Cancellation (AHC)*. From this theory, two implementation variants are formulated: 1) *Continuously Adapted Harmonics Cancellation (CAHC)* and 2) *Previously Adapted Harmonics Cancellation (PAHC)*. For realization of CAHC, an FPGA-implementation of narrowband ANC [6]-[8] has been transferred to EMC. Prior, an insight is given into the utilized FPGA-system regarding hardware capabilities and programming process. The performance and limitations of CAHC on the FPGA-system are investigated in regard to the suppression limits, the harmonic distortion and the frequency limits. The effectivity of the method is demonstrated for a dc-to-dc converter in an automotive component measurement setup. A conclusion closes the work.

II. STATE OF THE ART: ACTIVE FILTERS

Prior to introducing Adapted Harmonics Cancellation, the current state of the art for EMI cancellation is discussed: active filters. The discussion includes the fundamental topologies, the influence of the delay times on the achievable attenuation and further issues.

A. Topologies

In general, there are feedforward and feedback active filters [3], [4]. In both strategies, the active filter is set between EMI source and EMI sink and reduces the disturbances at the sink. Feedback-types detect the disturbances directly at the sink and inject a compensation signal for suppression. Feedforward-types measure the disturbances at the EMI source and inject the inverted signal for cancellation. In theory, feedforward active filters nullify the disturbances completely if EMI and anti-EMI are exact opposites of each other (phase-shift of 0° and inverted amplitude). In reality, the amplitudes cannot be exactly the same. Furthermore, all circuitry contains delays due to, e.g., the slew rates of semiconductors or the finite propagation speed of electromagnetic signals. As feedforward active filters theoretically offer infinite attenuations, they are considered in the following investigation.

B. Influence of the Delay Times

In this section, the impact of the unavoidable delay is analyzed. The assumed system is depicted in Figure 1. The EMI source generates the disturbance $y_{\text{EMI}}(t, f)$ that propagates through the active filter. The feedforward active filter detects $y_{\text{EMI}}(t, f)$ and ideally inverts the signal by a multiplication with -1 . This ideal signal is delayed by t_d and results in the

anti-EMI $\underline{y}_{\text{anti}}(t, f)$. EMI and anti-EMI are superposed to the resulting disturbance $\underline{y}_{\text{res}}(t, f)$.

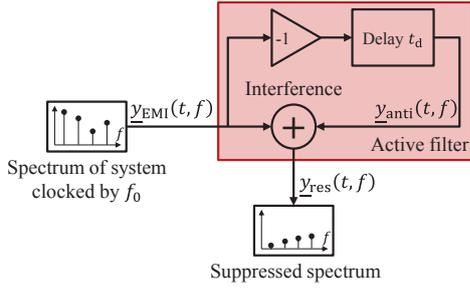


Figure 1: Structure of Feedforward Active Filters

Both, EMI and anti-EMI can be described by the complex phasors (1) and (2) with $A \in \mathbb{R}^+$:

$$\underline{y}_{\text{EMI}}(t, f) = A \cdot e^{j2\pi f \cdot t} \quad (1)$$

$$\underline{y}_{\text{anti}}(t, f) = -A \cdot e^{j2\pi f \cdot (t-t_d)} \quad (2)$$

The resulting disturbance is calculated by (3):

$$\underline{y}_{\text{res}}(t, f) = \underline{y}_{\text{EMI}}(t, f) + \underline{y}_{\text{anti}}(t, f) \quad (3)$$

To find the achievable reduction $\Delta Y(f)$, (4) is introduced:

$$\Delta Y(f) = 20 \text{ dB} \cdot \log_{10} \left(\frac{|\underline{y}_{\text{EMI}}(t, f)|}{|\underline{y}_{\text{res}}(t, f)|} \right) \quad (4)$$

Combining and transforming (1)-(4) leads to (5):

$$\Delta Y(f) = -10 \text{ dB} \cdot \log_{10}(2 \cdot [1 - \cos(2\pi f \cdot t_d)]) \quad (5)$$

Exemplary, for delay times of 1 ns, 10 ns and 100 ns, the achievable reductions are depicted in Figure 2. Smaller delay times result in higher reductions as the anti-EMI is better synchronized with the EMI. For higher spectral frequencies, the same delay time causes a more severe phase-shift. Therefore, EMI and anti-EMI drift apart and the achievable reduction drops. For $t_d = 100$ ns, there is a local maximum for 10 MHz that is, theoretically, infinite. In this case, the phase-shift is increased to 360° . If the signals are stationary, EMI and anti-EMI are in phase again and there is a perfect cancellation.

So, the delay of the circuitry is a limiting factor for, both, the achievable reduction and the suppressible frequency range. As the delay cannot be eliminated entirely, the injection of a measured disturbance is disadvantageous. Under the assumption of stationary operating systems, it is possible to synthesize the anti-EMI from sine waves with specific amplitudes and phases that are synchronized with the disturbing system. In this concept, delays of the canceller can easily be compensated by phase-shifts of the sine waves and, therefore, the cancellation can be improved widely. This is the basic idea of Harmonics Cancellation introduced in III.A.

C. Further Issues

Other issues of active filters are the limited number of possible configurations, the necessity of precise transfer functions for feedforward-types and stability problems for feedback-types. To

enable arbitrary topologies for Harmonics Cancellation, the theory is extended by an adaptive approach in III.B.

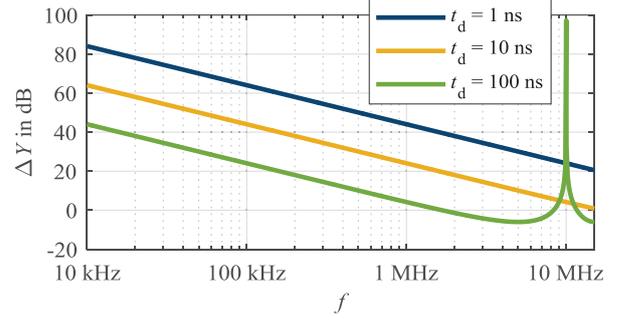


Figure 2: Achievable Reduction for Different Delay Times

III. THEORY

In this chapter, a specialized strategy for active cancellation of stationary clocked systems is derived: *Harmonics Cancellation* (HC). To easily and precisely find the necessary cancelling parameters for complex or even unknown systems, the method is extended by an adaptive approach to *Adapted Harmonics Cancellation* (AHC).

A. Harmonics Cancellation (HC)

Clocked systems, like power electronic converters, cause distinctive harmonics with a spacing of the fundamental frequency f_0 . To suppress the disturbances of such a system in a specific frequency range, only the harmonics must be eliminated. This is the basic idea of HC as depicted in Figure 3. By the application of HC, the first $K \in \mathbb{N}$ disturbing harmonics shall be cancelled out. For each harmonic $k \leq K$, a synthesizer generates a corresponding sine wave with such amplitude A_k and phase φ_k that there is a destructive interference for the specific frequency.

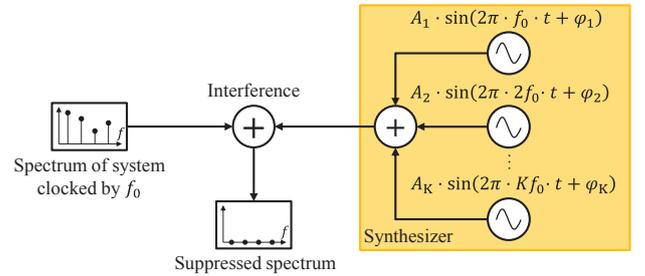


Figure 3: Principle of HC

B. Adapted Harmonics Cancellation (AHC)

In reality, there are often complex systems that are either time-consuming to describe (especially for high frequencies) or simply unknown. For a simple and effective parametrization of the sine waves, AHC (Figure 4) is introduced. In general, there are the presented synthesizer of anti-EMI and an unknown clocked system with a switching frequency of f_0 . The interference between the EMI and the anti-EMI causes a resulting spectrum that shall be reduced. To do so, an optimizer sets the amplitudes A_k and phases φ_k of the sine waves in such way that the feedback signal is minimized. In the simplest case, the optimizer could be a search algorithm. By this method, each sine wave is

optimized independently in its respective amplitude A_k and phase φ_k . So, there is no need to evaluate or construct complex transfer functions for a successful cancellation. Additionally, there are no limitations for the system's structure: By the simple parametrization of the sine waves, all bothersome unknown effects, like delays, phase-shifts or attenuations, can be compensated and, therefore, neutralized.

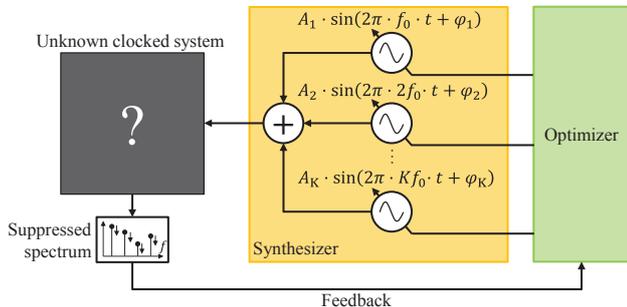


Figure 4: Principle of AHC

C. Comparison to Active Filters

On the one hand, AHC is a method that is specialized for the EMI cancellation of stationary clocked systems and enables the compensation of many effects (e.g. delay times or phase-shifts or attenuations) that limit the effectivity of active filters. On the other hand, active filters are not limited to stationary clocked systems. Therefore, they can be applied to non-stationary or even stochastic EMI sources with broadband characteristics. Despite the universal application of active filters, the feasible topologies are limited to some general structures [3], [4]. Due to the simple parameter correction of AHC, there are no restrictions regarding the realized topology. So, for stationary clocked systems, AHC has some advantages over active filters. Nevertheless, active filters can be applied to more classes of EMI sources.

IV. IMPLEMENTATION VARIANTS

There are many possible implementation variants to apply AHC to a clocked system. In this chapter, two elemental strategies are discussed: 1) *Continuously Adapted Harmonics Cancellation* (CAHC) and 2) *Previously Adapted Harmonics Cancellation* (PAHC). In this work, CAHC is applied.

A. Continuously Adapted Harmonics Cancellation (CAHC)

In CAHC (Figure 5), the cancellation signal is continuously adapted to the system. Again, there are the clocked system, the optimizer and the synthesizer for the cancellation signal. To find the feedback signal, the spectrum is measured by a sensor. This sensor consists, e.g., of a decoupling capacitor and an ADC. The cancellation signal is brought into the clocked system by an injector that consists of, e.g., a DAC and an inductive transducer. As the cancellation signal is adapted to the whole system, there are no restrictions for the structure of the injectors, sensors and clocked systems. For synchronization of the cancellation signal to the disturbances, the synthesizer is triggered by the clocked system. This trigger should be correlated to the disturbances and not eliminated by the cancellation. Control signals are especially convenient as they are highly correlated to the disturbances, easily measured and not influenced by the cancellation.

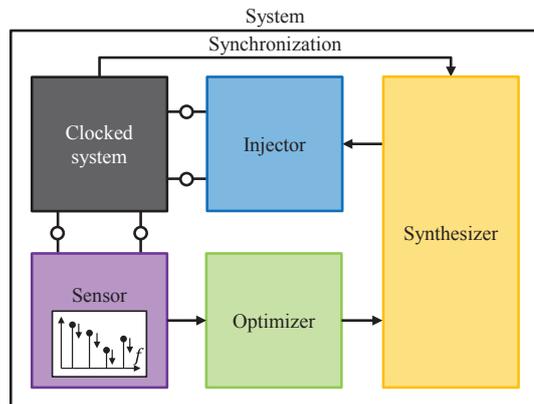


Figure 5: Continuously Adapted Harmonics Cancellation

B. Previously Adapted Harmonics Cancellation (PAHC)

To reduce the hardware requirements of the canceller, it is possible to outsource sensor, optimizer and partially the synthesizer into an external trainer. In this case, the canceller remaining in the system is provided with a memory to store the cancellation signals or parameters that were previously optimized by the trainer. In stand-alone operation, after removal of the trainer, the stored signals or parameters are sequentially read out and injected into the system. Of course, the canceller must be trained for all relevant operating modes of the clocked system as these determine the disturbing spectrum. Additionally, during stand-alone operation, the canceller must be informed about the current operating mode to inject the correct compensation signals into the system.

V. FPGA-IMPLEMENTATION OF CAHC

In this chapter, the used FPGA-system and its programming process are introduced. For this platform, the realized implementation of CAHC is depicted.

A. FPGA-System: Red Pitaya STEMLab 125-14

In this work, the FPGA-system Red Pitaya STEMLab 125-14 is used as a powerful and flexible development tool. The STEMLab 125-14 mainly consists of a System-on-Chip (SoC), two ADCs, two DACs and several GPIOs. The SoC includes a FPGA (Xilinx Zynq 7010 SOC) and a dual-core ARM Cortex A9 CPU running a Linux operating system which enables programming of the FPGA and communication via Ethernet. The two ADCs and the two DACs have a resolution of 14 Bit and a sample rate of 125 MS/s. Therefore, RF analog input signals can be passed through the analog frontend, digitalized by the ADCs and processed inside the FPGA while digital output signals can be handed over to the DACs and injected into the setup. The main reasons for using STEMLab 125-14 in the context of CAHC are the fast and precise ADCs and DACs as well as the flexibility given by the FPGA itself.

B. Programming Process

To minimize the development time, it is desirable to provide a convenient modeling environment and a fast processing of the necessary tool chain. Therefore, MATLAB Simulink is used as a development environment for the FPGA's logic which also enables a prior simulation of the functionality. Based on this

Simulink Model, HDL (Hardware Description Language) Models of the desired logic are generated by the HDL Coder. These HDL Models are embedded into a standard frame in Xilinx Vivado.

Based on a correct HDL description of the circuit, basically three steps are needed to realize logic on an FPGA: Firstly, during the synthesis step, a netlist of logic elements is generated based on the functional description in Verilog. Secondly, during the implementation step, the netlist is modified to fit the used FPGA and the maximum signal transit times are reviewed. If the timing constraints are fulfilled and the implemented design still meets its description, the implementation step should be successful. Thirdly, a bit stream is generated that includes all necessary information to configure the FPGA corresponding to the intended design.

In a further step, a binary file is generated based on the bit stream. This binary file can be transferred over LAN from the developer's computer to the STEmlab's Linux OS via a FTP connection. The transferred logic can comfortably be activated using a SSH remote connection to the Linux OS.

The tool chain has been automated by a batch file. Thus, after system design in Simulink, only one batch file needs to be executed to program the FPGA. Furthermore, to enable the development from several different computers without the need of a bothersome installation process, the needed development software has been installed on a Virtual Machine (VM) which can easily be transferred to other computers.

C. Implementation of CAHC

In Figure 6, an FPGA-implementation of CAHC is schematically depicted. The logic of the canceller is based on [7] and [8] and implemented on a Red Pitaya. This structure, known as *Adaptive Notch Filter*, is well established in Active Noise Control of acoustical phenomena [5]. In Figure 6, the cancellation structure for the k -th harmonic is shown.

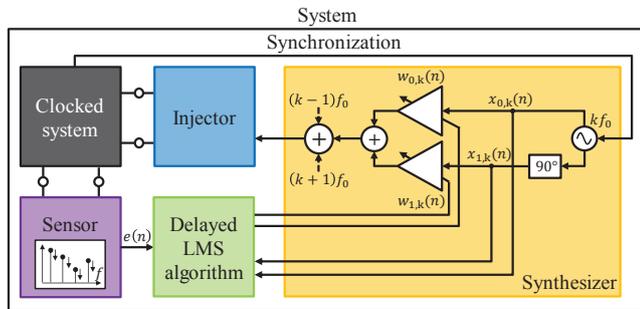


Figure 6: Implementation of CAHC

In this implementation, a sine wave $x_{0,k}(n)$ with the frequency kf_0 and an arbitrary amplitude and phase is generated. The sine wave is triggered by the synchronization signal and, therefore, correlated to the disturbances of the clocked system. To adjust the sine wave's amplitude A_k and phase φ_k , an orthogonal system is created by a phase-shift of 90° of the generated sine wave. Both, the original $x_{0,k}(n)$ and the phase-shifted signal $x_{1,k}(n)$ are respectively multiplied by the factors $w_{0,k}(n)$ and $w_{1,k}(n)$ and summated. By adjustment of these factors, any sine wave with the frequency kf_0 can be created. To suppress

multiple harmonics, the structure can be parallelized and the output signals can be superposed [5]. In Figure 6, the synthesized sine waves for the harmonics $k - 1$, k and $k + 1$ are summated.

To find the optimum sine wave, the delayed LMS algorithm is used [9], [10]:

$$w_{0/1,k}(n+1) = w_{0/1,k}(n) + \mu_k e(n) x_{0/1,k}(n - \Delta_k) \quad (6)$$

This algorithm basically compares the broadband error signal $e(n)$ with the generated signals $x_{0/1,k}(n)$ and adjusts the factors $w_{0/1,k}(n)$ to minimize the error. For the stability of the algorithm, the signals must be correlated in time. As DACs, ADCs and analog circuitries cause delays in the propagation of the signals, $e(n)$ is measured much later than $x_{0/1,k}(n)$ is generated. Therefore, the total delay Δ_k of the path from injecting to sensing is respected in the update rule (6) of the algorithm. The remaining variable μ_k is the step size of the algorithm. A large μ_k speeds up the convergence of the algorithm but may cause instability [11]. As there is a stationary operation of the system in this work, a very small μ_k is chosen for a precise adaption [12], [13].

VI. PERFORMANCE AND LIMITATIONS OF CAHC

In this chapter, the performance of CAHC on the Red Pitaya STEmlab 125-14 is evaluated. To do so, a simplified test setup is considered. For this setup, the suppression limits, the harmonic distortion and the frequency limits are discussed.

A. Test Setup

As a test setup, a simplified structure according to Figure 7 is investigated. For analysis purposes, the EMI should be controllable in amplitude and frequency. Hence, a singular sine wave is generated inside of the FPGA that acts as an artificial EMI. To limit the influence of parasitic effects, a simplistic power splitter is considered as the coupling system. As the EMI source and the coupling network are theoretically unknown, they are depicted as grey boxes. For cancellation, CAHC is implemented on the FPGA. Due to the same hardware platform, EMI and CAHC are intrinsically synchronized. The resulting disturbances are measured by a spectrum analyzer with an average detector.

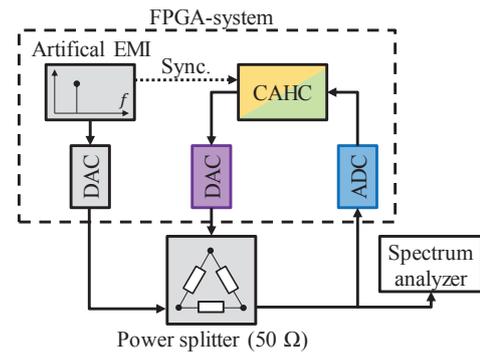


Figure 7: Test Setup (colors refer to prior figures)

B. Suppression Limits

In this section, the achievable suppression is investigated. Therefore, the artificial EMI's frequency is kept constant at 1 MHz and its level is varied. In Figure 8, measurements with and without CAHC are depicted. A resolution bandwidth of 9 kHz has been applied. Interestingly, all different harmonics

are suppressed to similar levels of 20 to 35 dB μ V. This is due to the noise floor of the ADC that limits the smallest measurable signals. Generally, there is the signal-to-noise ratio (SNR) that defines the quotient of the highest measurable sine wave and the noise floor, both in RMS values. For a sine wave and a quantization of m Bits, the SNR may be calculated by:

$$\text{SNR} = m \cdot 6.02 \text{ dB} + 1.76 \text{ dB} \quad (7)$$

For the quantization of 14 Bits, a SNR of approximately 86 dB results. As the ADC is limited to a voltage range of ± 1 V, a maximum sine wave with an RMS value of 117 dB μ V can be measured. So, the noise floor can be approximated to 31 dB μ V. In Figure 8, a good agreement is found between the residual disturbances with CAHC and the ADC's lower limit. So, the maximum achievable reduction is defined by the SNR of the ADC. For a specific suppression requirement, the necessary SNR and, therefore, the necessary number of Bits may be calculated by (7). In analogy, the DAC's SNR also limits the achievable reduction as it defines the quotient of the maximum producible sine wave and the noise floor, again in RMS values. Both, ADC and DAC should possess the same SNR to avoid a mutual limitation of the converters.

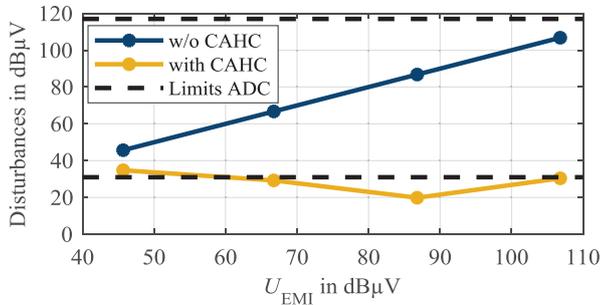


Figure 8: Measurement for the Achievable Suppression

C. Harmonic Distortion

Now, the harmonic distortion of the DACs is evaluated. In Figure 9, a measurement over a wide frequency range is depicted. For better visibility of the harmonics, a resolution bandwidth of 120 kHz has been chosen. In the spectrum without CAHC, there is the generated sine wave of 1 MHz. Due to the limited precision of the artificial EMI's DAC of 14 Bit, there is a harmonic distortion that generates harmonics at multiples of 1 MHz. With CAHC, the sine wave of 1 MHz is widely suppressed. Nevertheless, due to the CAHC's DAC, additional harmonic distortion is injected into the system.

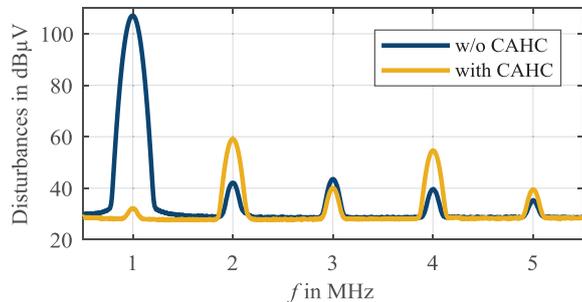


Figure 9: Measurement for the Harmonic Distortion

D. Frequency Limits

In the following, the frequency limits of CAHC for the considered FPGA-system are investigated. To do so, the artificial EMI's frequency is varied. The disturbances with and without CAHC are measured with a resolution bandwidth of 9 kHz and depicted in Figure 10. Independent of the considered frequency, the disturbances are reduced to at least the noise floor of the ADC. So, the effectivity of CAHC does not diminish for higher frequencies. Nevertheless, the sampling theorem limits the suppressible frequency range: As the STEMLab 125-14 utilizes a sample rate of 125 MS/s, frequencies of up to 62.5 MHz can theoretically be generated. However, as the in- and outputs have an analog bandwidth of 50 MHz, CAHC is limited to this frequency range for this FPGA-system.

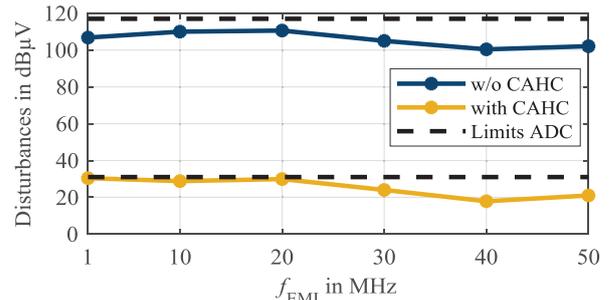


Figure 10: Measurement for the Frequency Limits

VII. DEMONSTRATION OF CAHC

In this chapter, CAHC is applied to a dc-to-dc converter as an example for a clocked system. At first, the demonstrator setup is introduced. Afterwards, measurement results are presented and discussed.

A. Demonstrator

The test setup is depicted in Figure 11. For demonstration, an evaluation board GS61008P-EVBBK is used to step down an input voltage of 48 V to 12 V for a resistive load of 1 Ω . The dc-to-dc converter is operated with a switching frequency f_0 of 300 kHz and a constant duty cycle of approximately 25 %. For demonstration, the disturbances of the primary side (48 V) shall be suppressed in respect to class 5 in the frequency range from 150 kHz to 1.8 MHz (LW, MW, [1]). As the converter operates with a switching frequency of 300 kHz, six harmonics must be cancelled out. For each of these harmonics, the structure depicted in Figure 6 is implemented on the FPGA-system Red Pitaya STEMLab 125-14.

For a measurement of the disturbances at the input of the converter, an artificial network is utilized. The disturbances are measured by the spectrum analyzer and, additionally, the FPGA-system. To avoid an overdrive of the FPGA-system's ADC by high-frequency disturbances, a low-pass filter with a cut-off frequency of 2.5 MHz is applied. For impedance matching, a 3 dB attenuator is connected in series. As injector, an inductive transducer is realized with a toroidal ferrite. The primary and secondary windings consist of two turns each. To block a possible DC-offset of the FPGA-system's DAC, a capacitor of 100 nF is connected in series. To achieve an inherent synchronization between the systems, the FPGA generates the

control signal for the transistors of the dc-to-dc converter. To avoid a corruption of the FPGA's measurement by ground loops, the control signal is passed through a digital isolator.

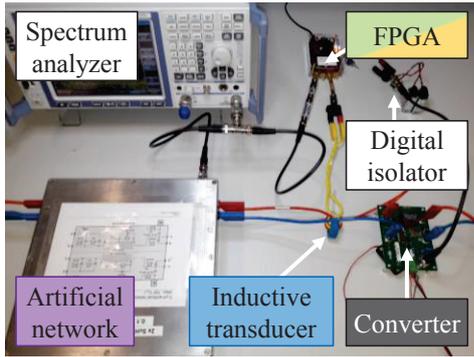


Figure 11: Demonstrator (colors refer to prior figures)

B. Measurement

In Figure 12, the average measurements with and without active CAHC are illustrated. According to [1], a resolution bandwidth of 9 kHz has been applied. In the considered frequency range, the cancellation suppresses the first six harmonics by respectively 66, 72, 50, 36, 47 and 48 dB. As intended, the system now complies with the class 5 limit.

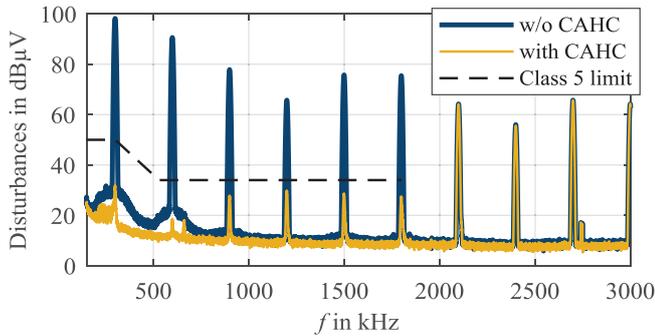


Figure 12: Average Emissions with and without CAHC

As investigated in VI.B, the harmonics are basically reduced to the noise floor of the ADC that has a level of 31 dB μ V. In contrast to VI.C, there is no harmonic distortion visible. This is due to the parallel structure of the canceller: The CAHC's sine wave of, e.g., 300 kHz injects harmonic distortion into the system that falls directly onto the subsequent disturbing harmonics. As these harmonics are also adaptively suppressed, the effect of harmonic distortion is compensated by the canceller itself. So, in regard to the cancellation signal, the harmonic distortion of the previous sine wave is compensated by subsequent sine waves. As the harmonic distortion is rather low compared to the disturbing harmonics, there is no significant influence on the spectrum over 1800 kHz.

In [14], the same test setup has been considered with worse results for CAHC. This was due to a jitter in the power transistors' control that limited the synchronicity of EMI and anti-EMI and the convergence of CAHC.

VIII. CONCLUSION

In this work, a specialized theory for the cancellation of stationary clocked systems' EMI was introduced: Harmonics Cancellation (HC) and Adapted Harmonics Cancellation (AHC). From this theory, the implementation variants Continuously Adapted Harmonics Cancellation (CAHC) and Previously Adapted Harmonics Cancellation (PAHC) have been derived. CAHC has been implemented on the FPGA-system Red Pitaya STEMLab 125-14. The FPGA-system has been presented regarding its hardware capabilities and the programming process. Additionally, the viability of CAHC has been shown for a wide frequency range that is only limited by the bandwidths of the in- and outputs and the sampling frequency. Furthermore, the ADC's and DAC's quantization has been found to be the limiting factor for the achievable EMI suppression of CAHC. The method has been applied to a dc-to-dc converter and measurements show its effectivity.

Currently, alternative implementation variants of AHC are investigated to reduce the hardware expenses of the system. Furthermore, there are ongoing studies on the systematic design of injectors and sensors.

REFERENCES

- [1] "CISPR 25 – Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers," 2015
- [2] P. Lueg, "Process of silencing sound oscillations," U.S. Patent 2 043 416, Jun. 9, 1936
- [3] N. K. Poon, J. C. P. Liu, C. K. Tse, M. H. Pong, "Techniques for input ripple current cancellation: classification and implementation," IEEE Trans. Power Electron., vol. 15, no. 6, pp. 1144-1152, Nov. 2000
- [4] Y.-C. Son, S.-K. Sul, "Generalization of active filters for EMI reduction and harmonics compensation," IEEE Trans. Ind. Appl., vol. 42, no. 2, pp. 545-551, Mar./Apr. 2006
- [5] S. M. Kuo, D. R. Morgan, "Active Noise Control: A Tutorial Review," Proc. IEEE, vol. 87, no. 6, pp. 943-973, Jun. 1999
- [6] B. Chaplin, "The cancellation of repetitive noise and vibration," Proc. Inter-noise, pp. 699-702, 1980
- [7] B. Widrow, J. R. Glover, J. M. McCool, J. Kaunitz, C. S. Williams, R. H. Hern, J. R. Zeidler, E. Dong, and R. C. Goodlin, "Adaptive noise canceling: Principles and applications," Proc. IEEE, vol. 63, no. 12, pp. 1692-1716, Dec. 1975
- [8] E. Ziegler, Jr., "Selective active cancellation system for repetitive phenomena," U.S. Patent 4 878 188, Oct. 31, 1989
- [9] G. Long, F. Ling, and J. G. Proakis, "The LMS algorithm with delayed coefficient adaptation," IEEE Trans. Acoust., Speech, Signal Processing, vol. 37, no. 9, pp. 1397-1405, Sep. 1989
- [10] G. Long, F. Ling, and J. G. Proakis, "Corrections to 'The LMS algorithm with delayed coefficient adaptation'," IEEE Trans. Signal Processing, vol. 40, no. 1, pp. 230-232, Jan. 1992
- [11] S. J. Elliott and P. A. Nelson, "Active noise control," IEEE Signal Processing Magazine, vol. 10, no. 4, pp. 12-35, Oct. 1993
- [12] D. R. Morgan, "An analysis of multiple correlation cancellation loops with a filter in the auxiliary path," IEEE Trans. Acoust., Speech, Signal Processing, vol. 28, no. 4, pp. 454-467, Aug. 1980
- [13] B. Widrow and S. D. Stearns, "Adaptive Signal Processing," Englewood Cliffs, NJ: Prentice-Hall, 1985
- [14] A. Bendicks, T. Dörlemann, S. Frei, N. Hees, M. Wiegand, "FPGA-basierte aktive Gegenkopplung der Schaltharmonischen von leistungselektronischen Systemen," EMV Düsseldorf, Düsseldorf, Germany, pp. 652-661, 20-22 Feb. 2018