EMI, Losses and Cooling of Low-Inductance GaN-HEMTs in a CCM PFC of an On-Board Charger

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Summary

This work deals with the usage of miniaturized low-inductance Gallium Nitride Power Transistors in the application of a CCM PFC of an On-Board Charger. The results are compared to a design with conventional semiconductor power devices. At first, the properties of GaN-HEMTs are shortly introduced. The chosen application is defined and explained. Next, the semiconductor losses are analyzed. These are put into relation to the cooling that is influenced by the miniaturized packages. After that, the conducted EMI is considered. These results are integrated to reveal the advantages and disadvantages of the technology of miniaturized GaN-HEMTs for the given application.

1 Introduction

Due to the special semiconductor properties, GaN-HEMTs (**H**igh-**E**lectron-**M**obility-**T**ransistor) may reduce conduction and switching losses in comparison to conventional power electronic devices. This is on account of lower resistances and steeper switching slopes as shown in e.g. [1]. These steep slopes require low parasitics, especially for higher switching frequencies [2]. Therefore, miniaturized low-inductance packages [3] and low-inductance PCB layouts [4] are a necessity.
There are many different investigations, e.g. [1][5][6][7], that show the improved efficiency of power converters if GaN-HEMTs are used. On the other hand, there are some analyses on the EMI of GaN-based power converters, e.g. [8][9][10].
This work pursues a holistic approach in which the semiconductor losses are put into relation to the cooling that is limited by the miniaturized packages. Additionally, the EMI is analyzed in regard to the switching noise and the coupling paths. These different results are integrated to uncover the advantages and disadvantages of miniaturized GaN-HEMTs.

2 Application

The chosen application is a **P**ower **F**actor **C**orrection (PFC) of an **O**n-**B**oard **C**harger (OBC). The OBC is used to charge the battery of a vehicle with energy drawn from the grid. The PFC consists of a full bridge rectifier and a boost converter. The full bridge rectifier converts the AC supply voltage into a pulsed voltage that consists of only positive half-waves. This voltage is the input for the boost converter. Ideally, the boost converter draws an in phase sinusoidal current from the AC supply (230 V, 50 Hz) enabling a power factor of 1. The PFC delivers a constant intermediate circuit voltage of 400 V.
There are a boundary conditions for the application: The OBC and thus the PFC shall supply 1.8 kW of electrical power. The device is liquid cooled and shall be able to supply full power at a coolant temperature of 70 °C.
For a comparison of the semiconductor technologies, two different designs are considered:
The first design (**Figure 1**) is a reference consisting of the Silicon Superjunction MOSFET IPW65R110CFDA (CoolMOS) in TO-247 and the **Si**licon **C**arbide (SiC) Schottky Diode SCS208AG in TO-220. CeraLink Capacitors with 1 µF have been used to realize the capacitances depicted in the figure. The switching frequency is 100 kHz.

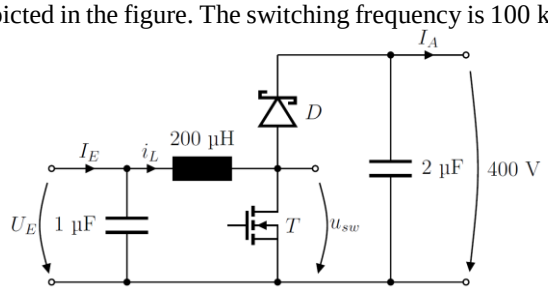

Figure 1: Boost converter with conventional semiconductors

The second design (**Figure 2**) consists of two GaN-HEMTs of the type GS66508T in miniaturized packages in order to reduce the loop inductance of the switching cell. Again, CeraLink Capacitors with 1 µF have been utilized and a switching frequency of 100 kHz has been chosen.

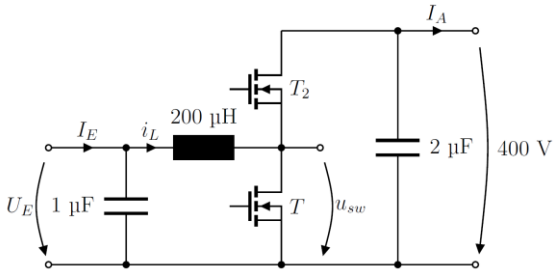

Figure 2: Boost converter with GaN-HEMTs

For better understanding, **Figure 3** shows a comparison between the miniaturized GS66508T and the package TO-247.

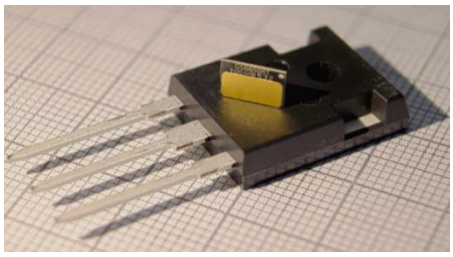

Figure 3: Miniaturized GS66508T on top of TO-247 (Source: GaN Systems)

In [11] it has been shown that the reference design has a loop inductance of approximately 41 nH while the GaN-HEMT variant only causes about 5 nH. Thus, the parasitic inductance of the switching cell is vastly reduced by the miniaturized packages of the GaN-HEMTs. As stated above, this reduction is recommended in order to limit the parasitic influences due to the steep switching slopes of GaN-HEMTs.

To explain the mode of operation of the PFC, a typical profile of the inductor current i_L is illustrated in **Figure 4**. i_E is the ideal sinusoidal current that shall be drawn from the grid. A **C**ontinuous **C**onduction **M**ode (CCM) is assumed in which the inductor current never drops to zero. Due to the switching nature of the boost converter, the ideal profile can only be approximated. If the transistor T is closed, the coil gets magnetized by the grid and the current rises. If the transistor T is opened, the current commutates to the output. The stored energy is delivered to the intermediate circuit and the coil current drops. The resulting ripple can be minimized by the usage of e.g. higher coil inductances or higher switching frequencies.

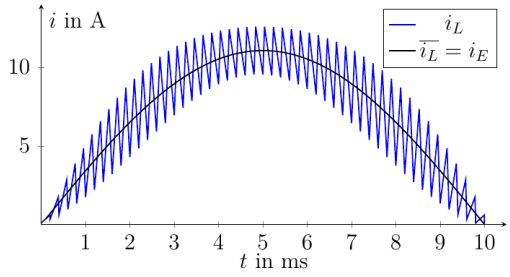

Figure 4: Current profile of the PFC

The switching of the transistor T causes a PWM-signal as depicted in **Figure 5**. It can be noticed that the duty cycle d changes during a half-wave of the mains. As discussed later on, this switched voltage is the source for the EMI of the system. Hence, detailed knowledge of the profile is essential.

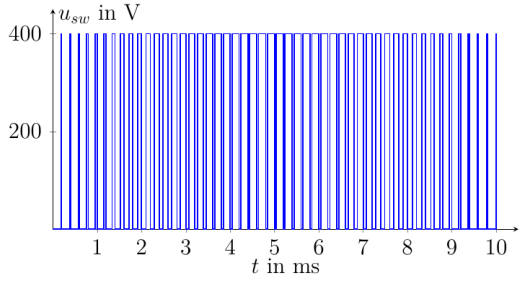

Figure 5: Profile of the switched voltage

3 Semiconductor Losses

The losses of semiconductor power devices can be divided into conduction, switching and C_{OSS}-losses. In this consideration, the focus lies on the switching transistor T.

3.1 Conduction Losses

A fully turned on transistor has a remaining resistance $R_{DS(on)}$. This resistance causes conduction losses if there is a current flowing through the device. In general, these losses may be calculated by the following formula [2]:

$$P_{cond} = R_{DS(on)} \cdot I_{DS,rms}^2$$

In case of a boost converter in CCM, the transistor losses of a single switching period may be calculated by [2]:

$$P_{cond,T} = R_{DS(on)} \cdot \left(\overline{i_L}^2 + \frac{(\Delta I_L)^2}{12} \right) \cdot d$$

As shown in **Figure 4** and **Figure 5**, $\overline{i_L}$, ΔI_L and d change over the period of the grid voltage. Thus, the conduction losses are calculated for each switching period and averaged over a grid period.

For the $R_{DS(on)}$ of both transistors, the worst case values (at junction temperatures of 150 °C) of $R_{DS(on),CoolMOS} = 257\ \text{m}\Omega$ [12] and $R_{DS(on),GaN} = 140\ \text{m}\Omega$ [13] are assumed.

In the application of the PFC, conduction losses of $P_{cond,CoolMOS} \approx 5.0\ \text{W}$ and $P_{cond,GaN} \approx 2.7\ \text{W}$ result. So, the conduction losses of T are approximately halved if the GaN-HEMT is used for the application.

3.2 Switching Losses

In hard switching events like in the considered boost converter, there are overlaps of current and voltage for the switching transistor (**Figure 6**):

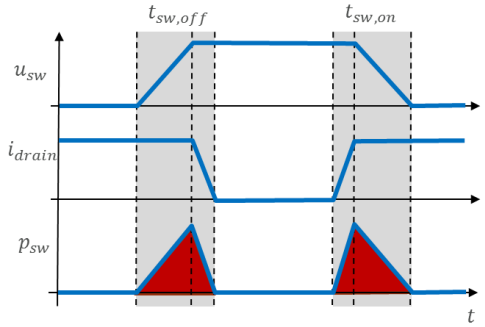

Figure 6: Typical switching behavior of MOSFETs

The times $t_{sw,on}$ and $t_{sw,off}$ depend on the driver voltage U_{DR}, the gate resistor R_{gate} and the properties of the transistor. These times can be separated into **V**oltage/**C**urrent **R**ise/**F**all times:

$$t_{sw,on} = t_{VF} + t_{CR}$$
$$t_{sw,off} = t_{VR} + t_{CF}$$

The following formulas describe the switching times of GaN-HEMTs [2]:

$$t_{VF} = \left(R_{gate} + R_{gate,int}\right) \cdot \frac{Q_{GD}}{U_{DR} - U_{pl(op)}}$$

$$t_{CR} = \left(R_{gate} + R_{gate,int}\right) \cdot \frac{Q_{GS2}}{U_{DR} - \frac{1}{2}\left(U_{pl(op)} + U_{th}\right)}$$

$$t_{VR} = \left(R_{gate} + R_{gate,int}\right) \cdot \frac{Q_{GD}}{U_{pl(\,op)}}$$

$$t_{CF} = \left(R_{gate} + R_{gate,int}\right) \cdot \frac{Q_{GS2}}{\frac{1}{2}\left(U_{pl(op)} + U_{th}\right)}$$

$$Q_{GS1} = \frac{Q_{GS}}{U_{pl}} \cdot U_{th}$$

$$Q_{GS(op)} = \frac{Q_{GS}}{U_{pl}} \cdot U_{pl(op)}$$

$$Q_{GS2} = Q_{GS(op)} - Q_{GS1}$$

$U_{pl(op)}(I_D)$ depends on the operating point of the transistor and is determined by the transfer characteristic $I_D(U_{GS})$. Due to this dependency, the switching times need to be calculated for each switching instance.

In the application with the values given in the datasheet [13], $U_{DR} = 7\ \text{V}$ and $R_{gate} = 5\ \Omega$, the average switching times of $t_{VF} = 2.4\ \text{ns}, t_{CR} = 0.6\ \text{ns}, t_{VR} = 5.3\ \text{ns}$ and $t_{CF} = 2.1\ \text{ns}$ are calculated for the GaN-HEMT.

Due to the complexity of the superjunction technology, the Voltage Rise and Fall times of CoolMOS transistors cannot be calculated by the formulas stated above [14]. Thus, the values of datasheet [12] have to be assumed: $t_{VF} = 11\ \text{ns}$, $t_{VR} = 6\ \text{ns}$. According to [15], the current rise and fall times can still be calculated by the formulas stated above. With $U_{DR} = 15\ \text{V}$ and $R_{gate} = 7.5\ \Omega$, the average times $t_{CR} = 4.3\ \text{ns}$ and $t_{CF} = 10.3\ \text{ns}$ result.

Thus, the GaN-HEMT offers much steeper switching slopes than the CoolMOS.

The switching losses are calculated by the following formulas [2]:

$$P_{sw,on} = \frac{1}{2} \cdot U_{DS} \cdot I_D \cdot t_{sw,on} \cdot f_{sw}$$

$$P_{sw,off} = \frac{1}{2} \cdot U_{DS} \cdot I_D \cdot t_{sw,off} \cdot f_{sw}$$

$$P_{sw} = P_{sw,on} + P_{sw,off}$$

U_{DS} equals the intermediate voltage of 400 V. I_D, $t_{sw,on}$ and $t_{sw,off}$ have to be calculated for each switching event. In the considered application, the losses of the transistors can be calculated to $P_{sw,GaN} \approx 1.6\ \text{W}$ and $P_{sw,CoolMOS} \approx 4.6\ \text{W}$. Hence, the switching losses are widely reduced by the usage of the GaN-HEMT.

It is notable that $P_{sw,off}$ may be halved for both variants because of the snubber effect of the output capacitances C_{OSS} [15].

3.3 C_{OSS}-Losses

Semiconductor devices carry parasitic output capacitances C_{OSS} that need to be recharged during the switching events. During the turn-on process of T, $C_{OSS,T}$ is discharged through T. Respectively, $C_{OSS,T2}$ and $C_{t,D}$ are charged by the intermediate circuit through T. These recharging currents cause C_{OSS}-losses in T.

During the turn-off process of T, the commutation drives the recharging of the output capacitances: $C_{OSS,T}$ is charged, $C_{OSS,T2}$ and $C_{t,D}$ are respectively discharged by the inductor current i_L. This process causes no additional losses in T.

Due to the nonlinearity of C_{OSS}, the stored energy E_{OSS} (at $U_{DS} = 400\ V$) is applied to calculate the losses: $E_{OSS,CoolMOS} = 9{,}2\ \mu\text{J}$ [12], $E_{t,Diode} = 2.6\ \mu\text{J}$ [16] and $E_{OSS,GaN} = 7.0\ \mu\text{J}$ [13].

The following formulas [2] are used:

$$P_{OSS,CoolMOS} = f_{sw} \cdot \left(E_{OSS,CoolMOS} + E_{t,Diode}\right) \approx 1{,}2\ \text{W}$$

$$P_{OSS,GaN} = 2 \cdot f_{sw} \cdot E_{OSS,GaN} \approx 1{,}4\ \text{W}$$

It can be seen that the C_{OSS}-losses are slightly increased if GaN-HEMTs are used.

It is possible to use a GaN-HEMT as T and a SiC-diode as D in order to reduce the C_{OSS}-losses. In this case, the SiC-diode should also be in a low-inductance package, so that the loop inductance of the switching cell is not increased.

3.4 Total Losses

The loss components of the transistors are summarized in **Table 1**. Due to the usage of the GaN-HEMT, the total losses P_{total} of the transistor are nearly halved.

	CoolMOS	GaN-HEMT	Alteration
P_{cond}	5.0 W	2.7 W	-46 %
P_{sw}	4.6 W	1.6 W	-65 %
P_{OSS}	1.2 W	1.4 W	+17 %
$\boldsymbol{P_{total}}$	**10.8 W**	**5.7 W**	**-47 %**

Table 1: Loss components of the transistors

4 Semiconductor Cooling

In operation, the semiconductors need to be cooled. Therefore, the thermal tabs of the semiconductor packages are thermally connected to a heatsink. In this application, liquid cooling and aluminum housing are used. The thermal tabs of the semiconductors are not electrically isolated from the circuit. Therefore, an electrical isolator with a thermal conductivity is needed – a **T**hermal **I**nterface **M**aterial (TIM). The system is illustrated in **Figure 7**.

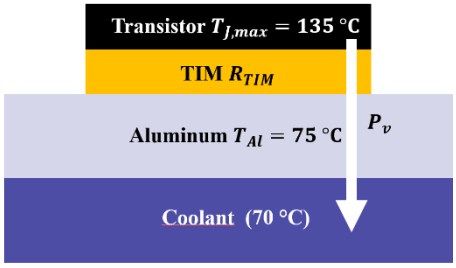

Figure 7: Cooling of the semiconductors

The maximum junction temperatures of the semiconductors are chosen to $T_{J,max} = 135\ °\text{C}$. Additionally, the coolant may have a temperature of 70 °C while the device supplies full electric power. It is estimated that the aluminum housing has a temperature of $T_{Al} \approx 75\ °\text{C}$.

The foil PC03-MT-100 [17] is chosen as TIM. It has a thickness d_{TIM} of 100 µm +/-15 µm and a thermal conductivity of about 1.6 W/mK. It is assumed that $R_{TIM,CoolMOS}$ equals 1 K/W. This value covers both the heat conduction through the TIM and the heat transfers in and out the TIM. This assumption is scaled to the GaN-HEMT. The thermal tabs have areas of $A_{CoolMOS} \approx 161.7\,\mathrm{mm}^2$ and $A_{GaN} \approx 19.5\,\mathrm{mm}^2$. The thermal resistance $R_{TIM,GaN} \approx 8.3$ K/W follows from the proportionality $R_{TIM} \propto 1/A$.
The thermal circuit can be described by **Figure 8**. R_{JC} is the thermal resistance from the junction to the case of the transistors. The semiconductor losses are represented by P_v.

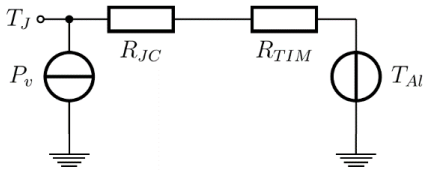

Figure 8: Thermal circuit

Therefore, the maximum permitted losses can be calculated by:

$$P_{v,max} = \frac{T_{J,max} - T_{Al}}{R_{JC} - R_{TIM}}$$

Under consideration of $R_{JC,CoolMOS} = 0.45$ K/W [12] and $R_{JC,GaN} = 0.5$ K/W [13], the values $P_{v,max,CoolMOS} \approx 41.4$ W and $P_{v,max,GaN} \approx 6.8$ W follow. It is obvious that the miniaturized package of the GaN-HEMT massively delimits the allowed semiconductor losses.
Nevertheless, both CoolMOS and GaN-HEMT produce reasonable losses of respectively 10.8 W and 5.7 W that fall below the cooling limits. It is notable that the GaN-HEMT is much closer to its thermal limit than the CoolMOS.

5 EMI

5.1 Model for Conducted EMI

In this chapter, the conducted EMI of the PFC shall be predicted. According to [18] and [19], a simplified model (**Figure 9**) is used.

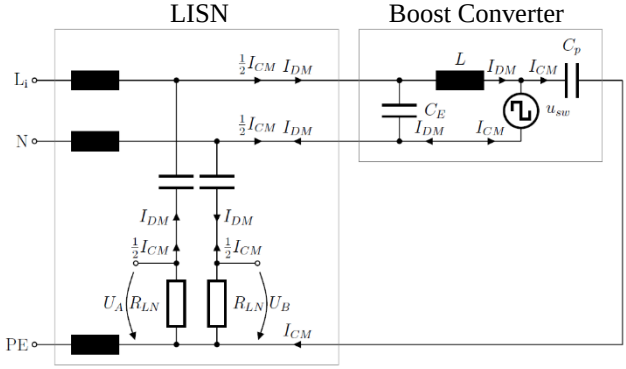

Figure 9: Model for the conducted EMI of the PFC

The boost converter of the PFC is simplified to a pulsed voltage source u_{sw}, the inductor L and the input capacitor C_E. Furthermore, there is a coupling capacitance C_p between the switching node and the housing that is itself electrically connected to PE.
C_p results from the thermal circuit of the semiconductor devices: The thermal tabs, the TIM and the aluminum housing form a capacitance. As mentioned above, the thermal tabs are electrically connected to the circuit.
For the CoolMOS, the thermal tab is connected to drain and thus to the switched potential. On the other hand, the thermal tab of the SiC-diode is tied to the cathode and so connected to the fixed high potential of the intermediate circuit. This means that only the thermal tab of the CoolMOS acts as a coupling capacitance for this design variant.
The thermal tab of the GaN-HEMT is tied to source. So, the thermal tab of the low-side GaN-HEMT is connected to the fixed low potential of the intermediate circuit. Therefore, the thermal tab of the high-side GaN-HEMT is connected to a switched potential and so contributing to the coupling capacitance of the variant.
The coupling capacitance is estimated by the following formula:

$$C_p = \varepsilon_{r,TIM}\varepsilon_0 \cdot \frac{A}{d_{TIM}}$$

With $\varepsilon_{r,TIM} = 4.5$ [17], $d_{TIM} = 85$ µm [17], $A_{CoolMOS} \approx 161.7\,\mathrm{mm}^2$ and $A_{GaN} \approx 19.5\,\mathrm{mm}^2$, the capacitances $C_{p,CoolMOS} \approx 76$ pF and $C_{p,GaN} \approx 9$ pF follow.
It is obvious, that the smaller thermal tab of the GaN-HEMT vastly reduces the coupling capacitance from the switching node to the housing.

5.2 Spectrum of the Source u_{sw}

As stated above, the switched voltage u_{sw} is the noise source of the system. In **Figure 10** the FFT of u_{sw} is illustrated for both CoolMOS and GaN-HEMT.

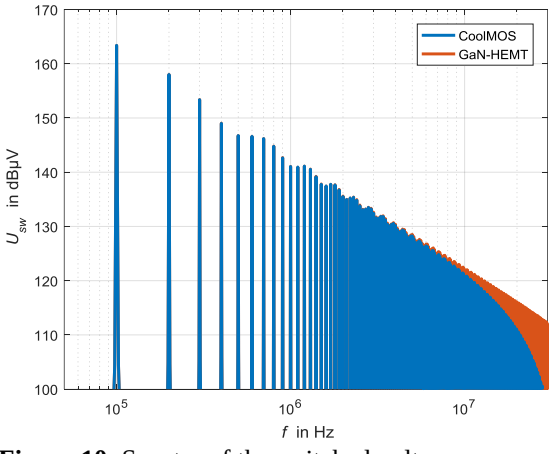

Figure 10: Spectra of the switched voltages u_{sw}

In the spectra, the switching frequency of 100 kHz and its harmonics can be seen. At first, the spectra drop with 20 dB/decade [20]. For low frequencies, both spectra are the same due to the same point of operation. After a frequency of $1/(\pi \cdot \tau_r)$, the spectra drop respectively with

40 dB/decade [20]. τ_r is the rise and fall time of an ideal trapezoidal waveform. As seen before, the GaN-HEMT has steeper slopes and thus a shorter time τ_r. Therefore, the spectrum of the CoolMOS drops at lower frequencies with 40 dB/decade reducing its EMI at higher frequencies.
So, the switching waveforms of the GaN-HEMT produce more EMI for high frequencies but not for the first harmonics.

5.3 Differential Mode EMI

Following the differential mode currents I_{DM} of **Figure 9**, the simplified circuit of **Figure 11** results [18].

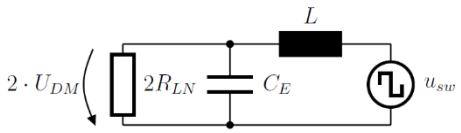

Figure 11: Model for differential mode EMI

It can be seen that only L, C_E and $R_{LN} = 50\,\Omega$ contribute to the transfer function of the system [18]:

$$U_{DM} = \frac{R_{LN}}{2R_{LN}(1-\omega^2 LC_E) + j\omega L} \cdot U_{sw}$$

With the usage of the calculated spectra of the source, the differential mode disturbances can be calculated to (**Figure 12**):

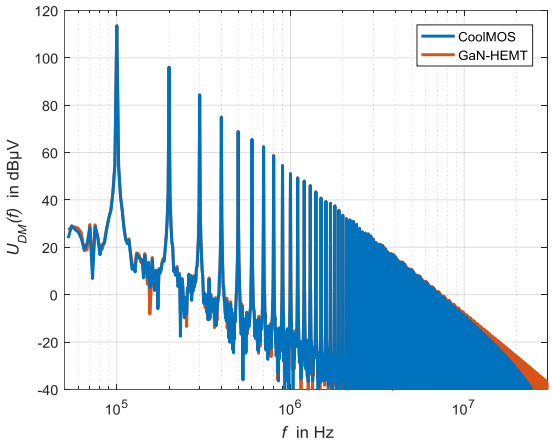

Figure 12: Differential mode EMI of the PFC

Both variants produce nearly the same differential mode EMI. This is due to the fact that the transfer functions are identical. There is only a deviation for the high frequency spectra due to the different slopes of the transistors.
The transfer characteristic for the differential mode acts as a second order low-pass filter. Thus, the transfer function drops with 40 dB/decade [18]. In superposition with the decrease of 20 dB/decade for the source spectra, the differential mode EMI falls with 60 dB/decade.

5.4 Common Mode EMI

The simplified model for the common mode EMI is depicted in **Figure 13** [18].

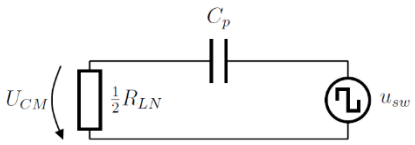

Figure 13: Model for common mode EMI

It is obvious that only C_p and $R_{LN} = 50\,\Omega$ influence the transfer function [18]:

$$U_{CM} = \frac{j\omega C_p R_{LN}}{j\omega C_p R_{LN} + 2} \cdot U_{sw}$$

The common mode EMI illustrated in **Figure 14** results from the transfer function, the calculated source spectra and the values of the coupling capacitances.

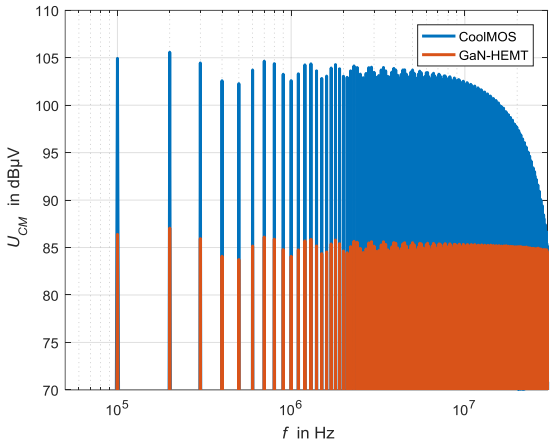

Figure 14: Common mode EMI of the PFC

It can be seen that the CoolMOS variant produces much more common mode noise than the GaN-HEMT design. This is due to the coupling capacitances that are much smaller for the GaN-HEMT.
For the common mode, the transfer characteristic acts as a first order high-pass filter. Its transfer function rises with 20 dB/decade [18]. In superposition with the drop of the source spectra of 20 dB/decade, flat spectra result for low spectral frequencies. For high spectral frequencies, the decrease of the source spectra of 40 dB/decade dominates and the spectra start to drop.

5.5 Total EMI

For the total EMI, common and differential mode disturbances are superposed:

$$U_A = U_B = U_{DM} + U_{CM}$$

The total EMI spectra are presented in **Figure 15**. For the switching frequency, the differential mode disturbances dominate due to the much higher level. So, both CoolMOS and GaN-HEMT produce nearly the same EMI. For higher frequencies, the influence of the differential mode decreases. Thus, the common mode disturbances become more prominent and the flat spectra are visible again.

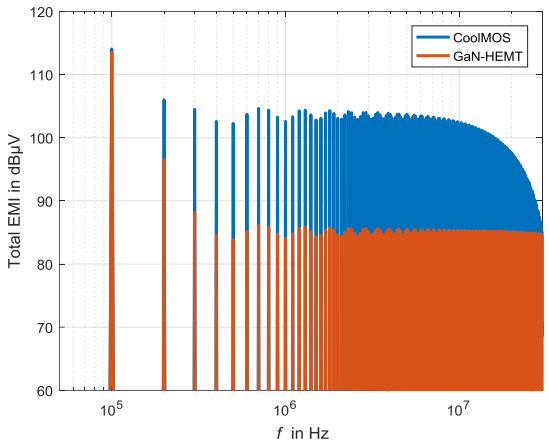

Figure 15: Total EMI of the PFC

Overall, it is clear that the GaN-HEMT variant produces less total EMI than the CoolMOS design. This is because of the much smaller thermal tab that results in a lower coupling capacitance. It is notable that this effect is due to the miniaturized package and not to the semiconductor material itself.

6 Conclusion

GaN-HEMTs need low-inductance packages to fully utilize the steep switching slopes of the semiconductor material. Due to this requirement, GaN-HEMTs are often built into special miniaturized packages.

These packages also involve smaller thermal tabs that limit the permitted semiconductor losses. While the considered CoolMOS in TO-247 may dissipate 41.4 W for the chosen application, this value is reduced to 6.8 W for the GaN-HEMT. This fact demands low-loss semiconductors.

For the application of a CCM PFC, it has been shown that the semiconductor losses are in fact reduced by the usage of GaN-HEMTs. The GaN-HEMT causes 5.7 W losses that are nearly the half of the CoolMOS losses of 10.8 W. Both semiconductors losses meet the thermal limits of the respective packages.

It has been shown that the smaller thermal tabs of the GaN-HEMT result in lower common mode disturbances and thus in lower conducted EMI overall. The reduction is nearly 20 dBµV for a wide frequency range.

All in all, GaN-HEMTs in miniaturized packages offer interesting advantages: The switching parasitics are reduced for a clean switching behavior. Furthermore, the smaller thermal tab causes a reduction of the conducted EMI. On the downside, the cooling of the devices is severely limited by the smaller thermal tabs. Additionally, GaN-HEMTs may produce more radiated EMI for high spectral frequencies due to the steeper switching slopes.

It is notable that the advantages listed above are mostly due to the miniaturized package and not due to the semiconductor properties of the GaN-HEMT. Nevertheless, a low-loss semiconductor material is a requirement for the utilization of these advantageous miniaturized packages.

7 Literature

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