Experimental Validation of the Generalized Accurate Modelling Method for System-Level Bulk Current Injection Setups up to 1 GHz

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***Abstract* – A small-signal model of an automotive system-level bulk current injection (BCI) setup developed with a generalized accurate method shown in the previous publication [3] is verified on a case study with a demonstrator EUT module. The work utilizes an equivalent circuit modelling approach for the floating ungrounded EUT board and a macromodel for an active DUT IC. The simulation-based prediction of the BCI test results using an IC failure threshold and a small-signal simulation of RF levels at floating EUT module under BCI tests is shown. Due to high accuracy and detail of the BCI setup model, the prediction also shows very good correlation to real measurement data, both qualitatively and quantitatively, up to 1 GHz.**

Keywords —Simulation of EMC tests, bulk current injection, floating non-grounded EUT module, VectFit macromodeling, common to differential mode conversion

I. INTRODUCTION

The simulation-based EMC analysis of ICs and EUTs and the virtualization of system- and IC-level EMC tests [1,2] are actively investigated by multiple research groups [4-9]. The possible approaches to define correlation of system-level and IC-level EMC tests are proposed. The methods have different names, but are mostly based on the characterization of EUT / DUT RF immunity with DPI at IC-level and simulation of equivalent RF disturbance in terms of RF voltage, current or power, delivered to EUT / DUT in a system-level test. The test result prediction is then performed by comparing the simulated RF disturbance level in a system-level test setup to a known IC failure threshold [4-9].

The approach sometimes shows good quantitative accuracy, but is also often used for simplified qualitative assessment of possible resonance locations without any expectation of quantitative fitting of the predicted results to real measurement.

A critical point of most investigations is the accurate model of the system-level EMC setups (e.g. Fig. 1) involving large-scale conducting structures like cable harnesses, field coupling to and from antenna structures and also floating ungrounded EUT modules. Several modelling methods were proposed for system-level setups, e.g. [4-13], including equivalent circuit modelling e.g. [11,12], 3D MoM or FEM simulations [13] and even measurement-based S-parameter-macromodeling [8,9], possibly indirectly involving VectFit methods [14-16].

A generalized accurate modelling method for automotive bulk current injection test setups valid up to at least 1 GHz was shown in [3]. The system-level BCI setup model is assembled on a modular basis. Each setup component starting with cable harness is characterized with VNA measurement and the equivalent circuit model is developed. The cable harness and metal fixtures are characterized with a very high accuracy, such that these can be used as deembeddable test fixtures for further component characterization. The BCI injection clamp with the clamped cable piece and the floating EUT board ground plane are characterized in this way.

The work [3] also proposes a combined macromodelling approach with LF equivalent-circuit-based extension of the measurement-based HF S-parameter data, by which the known issues of VectFit-based macromodels [17] are avoided. The transfer function (S_{mn}) from the RF port of the injection clamp to differential port at a passive RC load located at floating EUT board is reproduced with high accuracy up to 1 GHz.

The current work extends the test setup and model from [3] with a demonstrator EUT module. The floating ground plane modelling concept proposed in [18] and successfully verified in [3] is applied to the EUT board. The groundless differential monitoring concept using an optically-decoupled high-ohmic voltage probe and its effect on the result is discussed. The prediction based on characterization of the IC failure threshold using DPI setup and the small-signal simulation of the complete test setup model is presented.

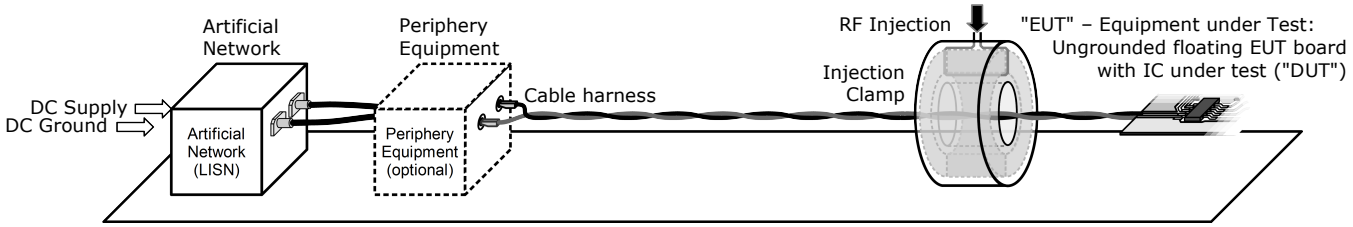

Fig. 1 Bulk current injection setup in open-loop configuration with a floating (non-grounded) EUT module

II. EUT Module, DUT IC, and Other Hardware

A. EUT module definition and structure

The EUT module used in current work consists of a linear voltage regulator IC (further "DUT") with minimal external circuitry sufficient for IC operation. The DUT IC is of a simple mass market type, and therefore doesn't include any specific built-in EMC protection. The device is used within this work to show the principles of the proposed modelling method, failure identification and system-level simulation.

The output pin is loaded with a 470Ω resistor R_L. The EMC capacitors are present at both supply and output pins (C_1 and C_3). An alternative capacitor location C_2 at supply pin allows increasing the ESL from 1.5 to 4.5 nH for analysis purposes.

The board layout (Fig. 2) is intentionally organized in a linear way from left to right side. With such configuration the dominating RF current flow direction in a BCI test setup would be longitudinal (along the main setup axis) for both CM and DM modes, which significantly simplifies the structure of the final model (section V.C). For complex layouts with significant lateral current components the models are more complex, but still can still be efficiently developed using 3D simulations.

The EUT module is supplied with 12 V DC voltage. The output level is measured over a low-pass RC filter located at the right PCB edge. No board connectors are intentionally used to keep the structure and the model as simple as possible. The traces are routed to the PCB edge and all external connections to the board, e.g. the cable harness in final setup, are soldered to the trace and ground edges. For device characterization purposes, e.g. VNA and DPI, an edge-type SMA connector is temporarily soldered to the same nodes.

B. Measurement instrumentation for ungrounded EUTs

In the system-level BCI test the EUT module is located in 50 mm over the reference ground plane. The measurements at such "floating" structure require specific instrumentation and measurement methods, noted in this section.

1) Groundless S-parameter measurements

The single-ended and differential mode VNA S-parameter measurements are successfully performed for the ungrounded floating nodes using a test fixture deembedding technique described in Fig. 9A-C in Section V of [3].

2) Groundless DC / LF signal measurement

The LF signal monitoring at the floating EUT is performed using an optically-decoupled high-ohmic probe (Fig. 4).

The probe requires a DC supply, which is commonly taken from the EUT board. This significantly affects the RF signal propagation over the ungrounded EUT board. To reduce the probe effect on the EUT, a set of battery adapters was designed (Fig. 5). The resulting structure is used as an active groundless high-ohmic differential probe.

The CM impedance of the probe also shows significant influence on the RF signal propagation over the floating EUT and therefore has to be considered. The probe is characterized with an S-parameter measurement from the floating pins of the powered-up probe to the reference ground plane. The extracted

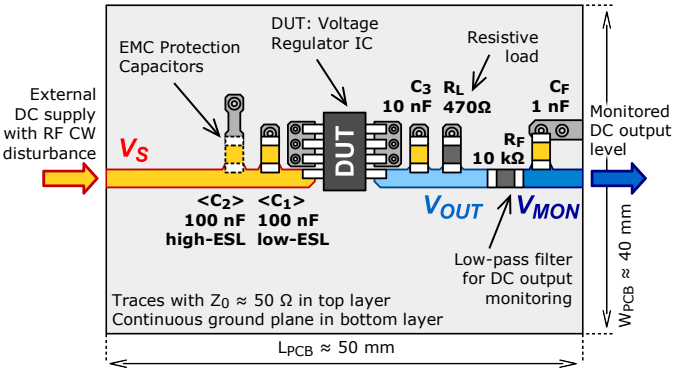

Fig. 2 Demonstrator EUT module: a voltage regulator IC (DUT) with minimal passive external circuitry at two-la yer 50×40 mm board

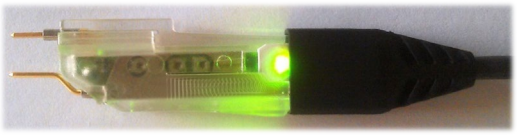

Fig. 3 Active high-frequency high-ohmic voltage probe
Range: ±12V DC ±8V Pk up to 2.5 GHz; C_{IN} ≈ 0.7 pF

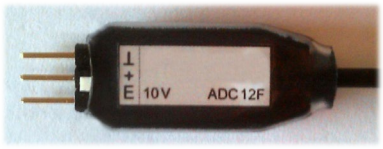

Fig. 4 Optically-decoupled low-frequency high-ohmic voltage probe
Range: 0 – 10 V with 12 bit ADC, BW 500 kHz, 3 MS/s
Pins: Reference, Supply (3 - 16 V DC, 30 mA), Input (C_{IN} ≈ 3.5 pF)

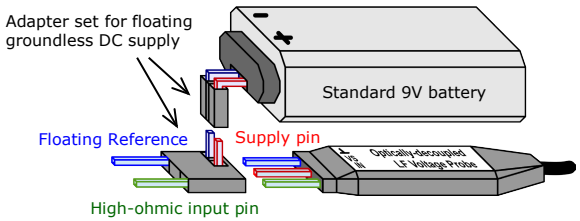

Fig. 5 Groundless DC supply concept for the optically-decoupled probe using a set of hand-made adapters to a standard 9V battery

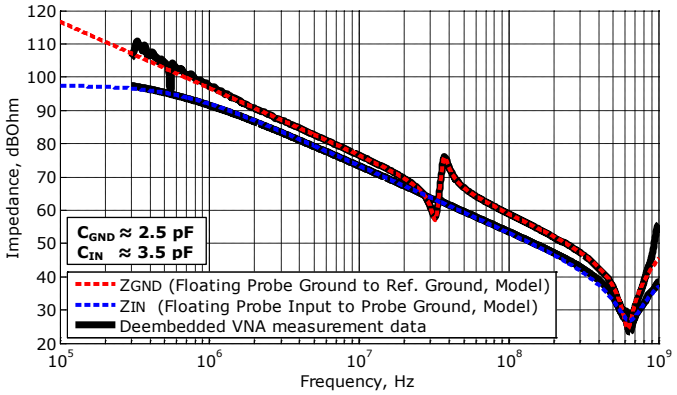

Fig. 6 Small-signal input impedances of a powered-up optically-decoupled probe located horizontally in 50 mm over main reference ground

impedances are modeled with equivalent RLC circuits, which are then included in the final setup model shown in Fig. 17. The modeled and measured impedances are shown in Fig. 6.

III. SMALL-SIGNAL DUT CHARACTERIZATION AND MODELLING

A. Small-signal DUT characterization

The modelling of integrated circuits for EMC simulation purposes is a separate complex topic. In many cases the DC shifts occur at the same RF amplitudes where the small-signal linear IC mode has barely been exceeded; therefore a linear small-signal RF wave propagation model of the DUT is often considered to be sufficient for RF level assessment purposes.

The DUT IC is characterized with a two-port S-parameter measurement. The DC supply and load are connected over bias tees outside the board and are included in the calibration path. The connectors and traces are deembedded up to IC pins; therefore the signal transfer over DUT is obtained as "from pin to pin" with a common reference ground for given bias and load conditions. The measurement is repeated for several RF power levels (-20 to 0 dBm with 1 dB step) to find the highest RF power level where the linear mode is still preserved.

B. VectFit approximation and macromodel generation

The S-parameter dataset is further processed with VectFIT approximation and the circuit macromodel is generated for the device as described in [14-17].

The final VectFit macromodel contains a rational function approximation of the original transfer function (S-parameter matrix) in a time-domain state-space model form, written-down in an equivalent circuit form using linear current and voltage control sources as operators and passive RC components as coefficients so, that it can be handled by a standard SPICE-like circuit simulator. The general structure of the model for a two-port S-parameter dataset is shown in Fig. 8.

The model reproduces exactly the same linear electrical behavior as captured with VNA, with possible measurement issues and approximation-caused artefacts. The LF equivalent circuit extension discussed in [3,17] is further applied used to avoid the measurement noise and possible data artefacts being approximated together with the original data. The measured and modeled S-parameters are shown in Fig. 9.

C. Model verification with lumped-pi-circuit decomposition

A good fitting of the S-parameters doesn't yet necessarily imply the overall quality of the linear circuit model [17]. To ensure the absence of the possible hidden measurement or approximation artefacts, the simulated and measured datasets are also compared in other ways, e.g. in admittance (Y) and impedance (Z) representations.

The lumped-pi-circuit decomposition can be effectively used for model verification (Fig. 10). The impedances from pins to ground ($Z_{IN1,2}$) show an RC profile with a high-ohmic resistive component parallel to approx. 20 pF capacitance. The transfer impedances ($Z_{TR21,\ 12}$) for a given non-passive dataset result to be different for two RF wave propagation directions (low-ohmic Z_{TR12} and high-ohmic Z_{TR21}). This data is used for additional macromodel verification (Fig. 11).

The VectFit macromodel shows good correlation to original measured dataset in most representations (S, Y and Z-parameters, lumped-pi-circuit impedances, etc.), and hence is considered to be of sufficient accuracy for current purposes.

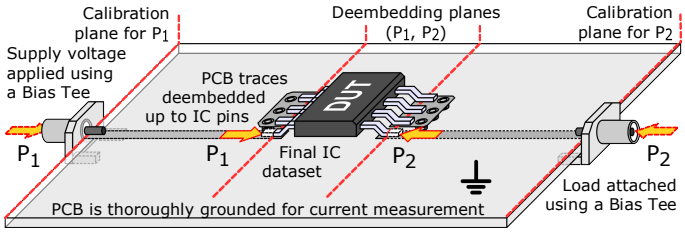

Fig. 7 Two-port VNA S-parameter characterization of the DUT IC

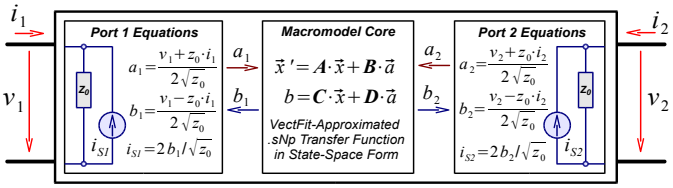

Fig. 8 Two-port S-parameter VectFit macromodel structure: ***x*** is a vector of internal variables (states), while ***A, B, C*** *and* ***D*** are the the coefficient matrices obtained by the original data approximation with VectFit

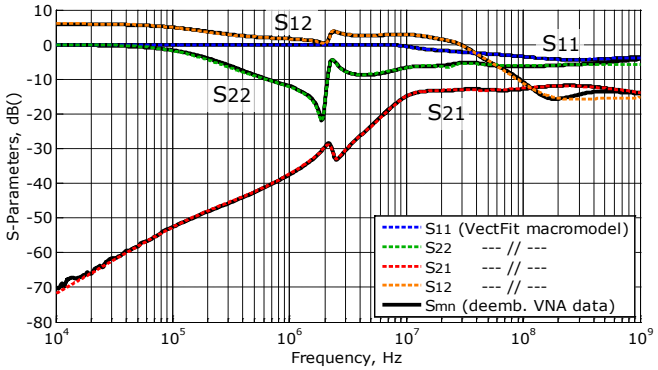

Fig. 9 Two-port S-parameter dataset of DUT IC (P_1 @ V_S, P_2 @ V_{OUT}) deemb. VNA measurement vs. S-parameter VectFit macromodel

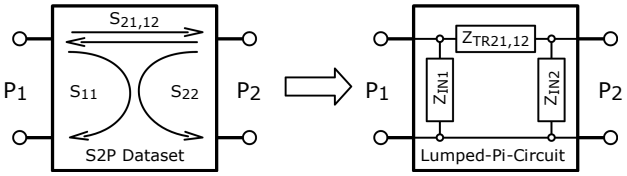

Fig. 10 Lumped-pi-circuit decomposition of the S-parameter dataset (impedances are used for model verification purposes only)

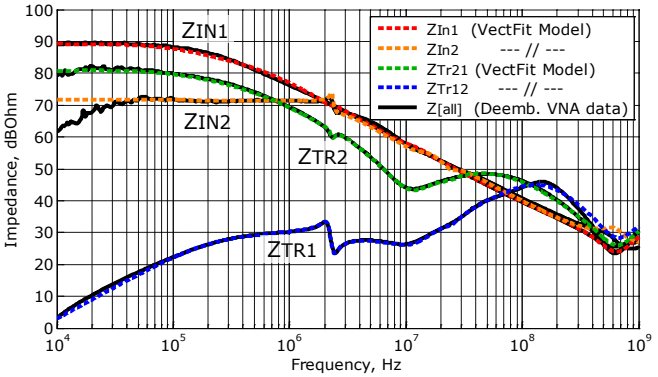

Fig. 11 Lumped-pi-circuit decomposition of DUT S-parameter dataset, deemb. VNA measurement vs. S-parameter VectFit macromodel

IV. DPI Characterization of DUT Failure Threshold

A. DPI setup and measurement procedure

The IC failure threshold is characterized with a customized DPI setup shown in Fig. 12. The PCB is thoroughly grounded. The standard coupling capacitor and DC inductor are not used; the RF wave is mixed with DC level using an external bias tee and injected into the PCB trace using an edge-type SMA port. The monitoring is performed over an RC low-pass filter. The IC pass state is defined as output voltage to be within ±100 mV in respect to its default value.

The measurement is repeated for two alternative blocking capacitor locations at supply node (C_1 of 100 nF with low ESL of 1.2 nH vs. C_2 of 10 nF with a relatively high ESL of 4.5 nH). Both results are shown in Fig. 13.

B. IC failure threshold extraction

The RF voltage amplitude at VS pin ($V_{VS\text{-}RF}$) is captured for each IC failure point using a high-frequency active probe shown in Fig. 3. The accuracy of this measurement method and its neglectable influence on the RF wave propagation were previously confirmed in [5].

The RF amplitude at VS pin is also estimated using a small-signal simulation model of the grounded EUT board. The model structure is identical to the upper part of the floating EUT board model shown in the next section (Fig. 17) with all PCB ground nodes connected directly to simulation reference.

The simulated RF signal amplitudes at VS pin fit to the measured data with good accuracy, therefore the validity of the measured and simulated data is considered to be confirmed.

The measured result shown in Fig. 14 shows, that in current case study for both configurations the IC failure (output DC shift over ± 100 mV) in the range from 10 MHz to 1 GHz can be observed at different RF power levels but for both cases at the same RF voltage amplitude at VS pin. The value varies in range from 0.4 to 1.2 V Pk depending on the frequency. Below 100 MHz the failure could only be reached in partial frequency range for a second "worse" location of a blocking capacitor. The IC failure threshold $V_{VS\text{-}RF\text{-}Fail}$ is defined for the continuous frequency using a smoothed linear interpolation of available data points vs. logarithmic frequency (Fig. 14).

V. Bulk Current Injection Test

A. BCI setup and measurement procedure

The BCI setup used for the measurement is derived from one described in detail in [3], with the same cable harness, BCI clamp and custom 1 GHz LISN. The only significant change in the final configuration is the EUT module (Fig. 16), which now includes an active DUT IC, passive SMD devices, and a probe.

The BCI measurement is performed with the same failure criteria as for DPI procedure, with a max. RF power limit of 47 dBm (available RF power amplifier capability).

B. BCI setup simulation model

The small-signal model of the BCI setup described in detail in [3] is used for modelling the RF wave propagation (in both CM and DM modes) up to the EUT board edge.

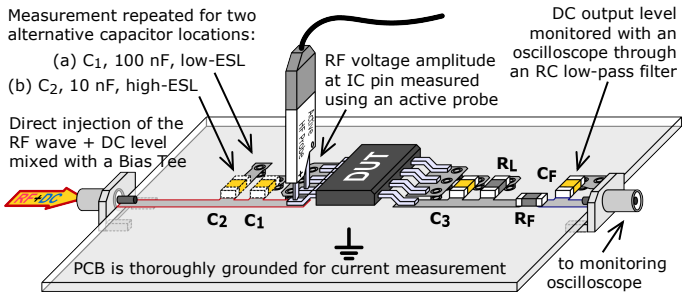

Fig. 12 Characterization of DUT failure threshold in a customized DPI setup

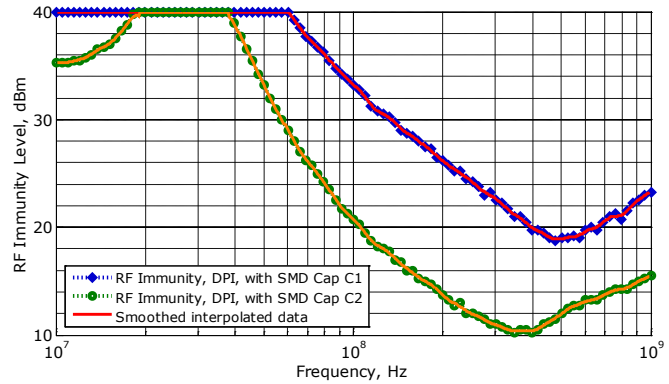

Fig. 13 DPI RF Immunity for two alternative blocking capacitors (C1, C2), measured in a customized DPI setup shown above

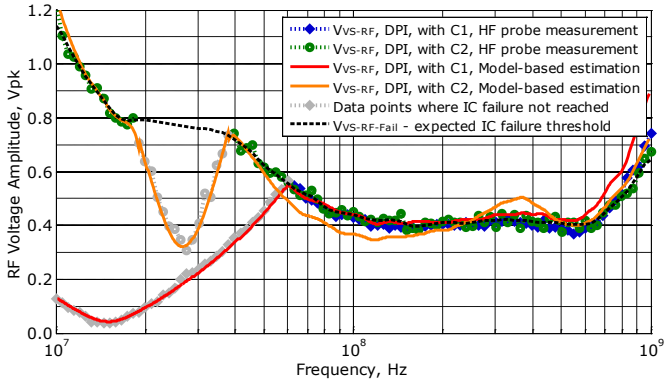

Fig. 14 DUT failure threshold in terms of RF amplitude at VS pin, measured with two alternative blocking capacitors locations and simulated using linear smallsignal models for given forward power level

C. Floating EUT simulation model

As shown in [18,19] and [3], the RF wave propagation along the longitudinal axis of the floating EUT board can be modeled with a multiconductor transmission line, where the floating PCB ground plane is considered to be just one more conductor over the main reference ground plane.

As long as the coupling of the top layer trace to the main reference ground can be neglected in comparison to the trace coupling to floating PCB ground, the model can be further decomposed into two independent TLs (trace vs. floating ground and floating ground vs. reference ground).

The TLs are defined in terms of per-unit-length RLCG parameters [21], which are characterized with VNA similar to [20]. The values are listed in Fig. 15.

PCB Trace:

L0	=	303 nH/m
C0	=	122 pF/m
R0	=	200 mΩ/m
G0	=	0 µS/m
RS	=	200 µΩ/m√Hz
GD	=	12.0 pS/Hz

Floating Ground:

R0	=	0 mΩ/m
L0	=	540 nH/m
C0	=	34 pF/m
G0	=	0 µS/m

Fig. 15 TL RLCG model parameters

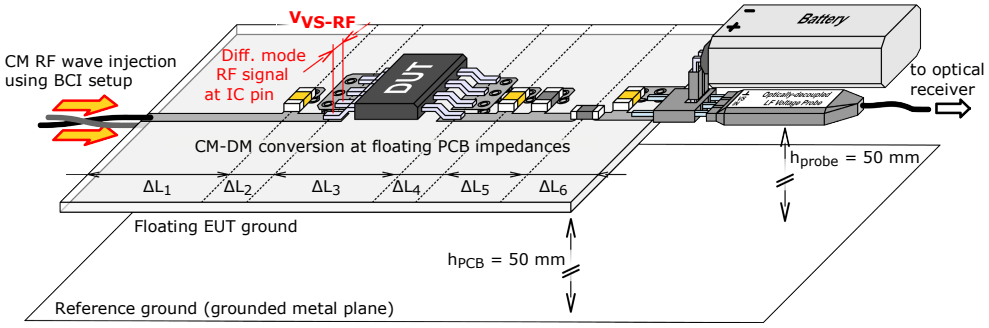

Fig. 16 Floating EUT board attached to cable harness in BCI test with optically-decoupled voltage monitoring

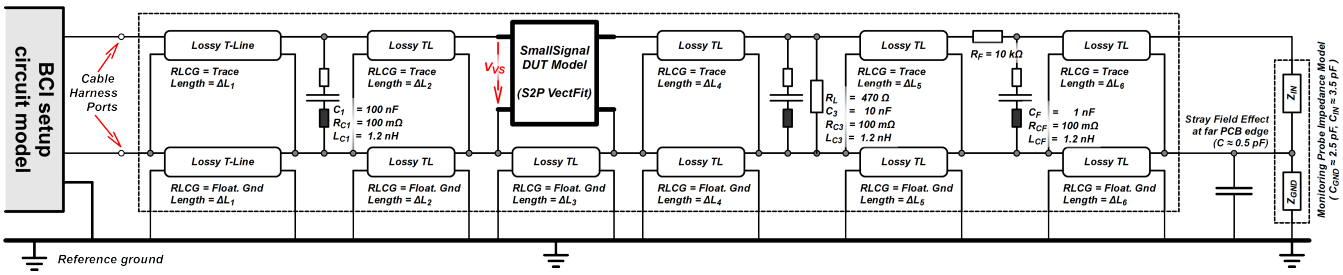

Fig. 17 Small-signal circuit model of the floating EUT board including stray field effect at far PCB edge and the effect of the attached monitoring probe

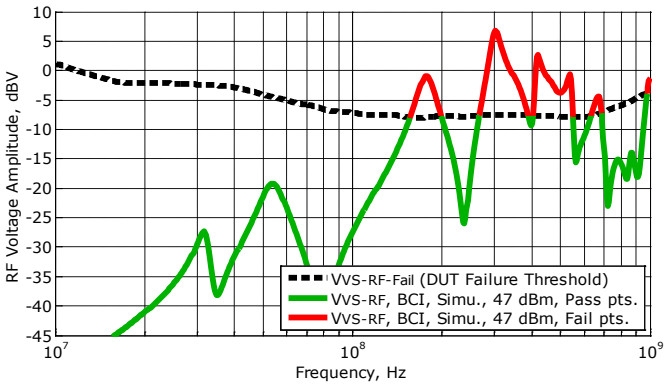

Fig. 18 Estimated RF amplitude at IC pin in Bulk Current Injection setup for a constant RF power of 47 dBm injected into BCI clamp

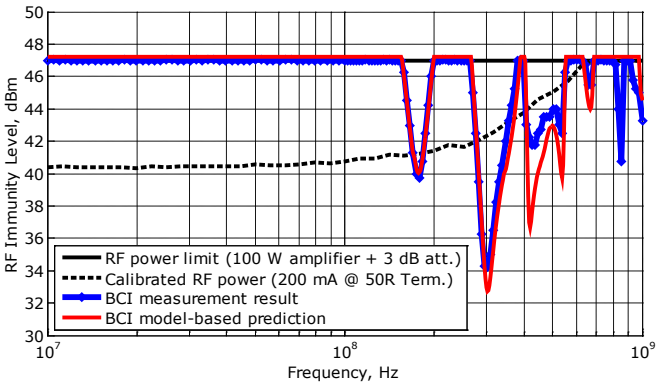

Fig. 19 EUT RF immunity measured using BCI setup and estimated using the simulated RF signal amplitude and DUT failure threshold

An interesting point could be derived from floating ground C_0 value. The total board capacitance to ground (for this board the value is 34 pF/m × 50 mm = 1.7 pF) significantly exceeds the simple flat capacitor estimation ($\varepsilon\varepsilon_0 \times wl/h \approx 0.35$ pF) due to significant stray fields to reference ground at PCB edges.

The passive components are modeled as equivalent circuits. The lateral RF wave propagation effects (e.g. the ESLs of SMD capacitors) are also included as lumped circuit elements.

Finally, the floating EUT model includes the effect of the stray field coupling to ground at far PCB edge (microstrip line open stub with a total capacitance of 0.5 pF) and the effect of the monitoring probe (approx. 2.5 and 3.5 pF, characterized in section II.B and modeled with simple equivalent circuits).

Despite its simplicity, this circuit model (Fig. 17) handles the CM-DM conversion with high accuracy. The signal transfer within the passive test setup part (with a series resistor instead of the IC to ensure the system passivity) is additionally verified with an S-parameter measurement (section II.B-1). The results show an extremely good correlation to measurement data very similar to the results in Fig. 15b in [3].

D. Model-based estimation procedure

The developed model (Fig. 17) can be used to calculate the RF signal amplitudes (voltages, currents, waves, etc.) at any node or through any branch of the system. The simulation in current work was performed with Synopsys HSPICE [21].

The RF voltage amplitude $V_{VS\text{-}RF}$ is simulated for a constant RF power of 47 dBm. The curve is plotted in Fig. 18 over the IC failure threshold. At the frequencies, where the estimated RF voltage exceeds the IC failure threshold, the failure in BCI test is expected. The EUT RF immunity in BCI test can be roughly estimated as the difference of $V_{VS\text{-}RF}$ to the IC failure threshold $V_{VS\text{-}RF\text{-}Fail}$ in dB scale. Such simplified prediction is shown in Fig. 19 together with the real BCI measurement data.

E. Results and discussions

An unexpectedly good correlation of the simulated and measured result is observed up to 400 MHz, both qualitatively and also quantitatively. In the further range up to 1 GHz the failure resonance locations and shapes are modeled with good accuracy, whereby the levels show differences up to 4-6 dB.

This deviation can be caused by a number of factors. The radiation losses, which are only included in a very simplified form within cable harness model, might damp the signal transfer to VS pin in the physical setup, resulting in a higher measured RF immunity. The IC failure threshold at VS pin might be affected by RF wave at other pins. The assumption on small-signal linear behavior of the system might become invalid due to a list of reasons. Still, the overall accuracy of the prediction, especially for the given setup configuration with a floating ungrounded EUT device, is considered to be very high.

The model has several significant limitations. Currently only the RF wave propagation along the setup main axis is handled by the model, while the lateral currents are modeled with simplified RLC circuits. This can be avoided by using a 3D MoM model of the floating ungrounded EUT board. Further investigations are currently performed at this point.

The prediction method based on IC failure threshold in terms of RF signal amplitude at IC pins can only be applied for analysis of known failures. The method was confirmed at this and several other case studies on simplified structures, but must be used with significant care, due of the high probability of side effects and additional unforeseen IC failure mechanisms.

The system-level test setup model of this accuracy can also be used in multiple other ways, i.e. for the search of critical current paths in floating EUT configurations or for the search and analysis of the resonance locations and levels for various floating nodes, even if the corresponding IC failure is not yet characterized. The modular structure of the final setup model makes it very effective for the device or component parameter variation and EUT board optimization.

The high-accuracy model can also be effectively used for the general analysis of system-level test setups, with a goal of localizing the relevant parameters at IC, EUT module, and system levels, which can be the reason of high differential RF disturbance levels in final application or in system-level tests, and developing the corresponding solutions at IC or EUT level.

VI. Conclusions

The generalized accurate modelling method for automotive system-level bulk-current injection test setups proposed in [3] was successfully verified on a demonstrator case study with a 50 × 40 mm floating EUT board containing an active voltage regulator IC (DUT) with minimal peripheral passive circuitry.

The CM to DM signal conversion at the floating board was successfully modeled using a TL-based equivalent circuit. All EUT component properties, especially the traces and floating ground per-unit-length RLCG parameters, were extracted from VNA measurements or estimated with alternative methods.

The DUT failure threshold was characterized in terms of RF voltage amplitude at its supply pin within a customized DPI setup. The RF disturbance level at the same node in a system-level test was simulated using the complete setup model and the expected RF immunity of the EUT in system-level BCI test was predicted. The results show a very good quantitative fitting up to 400 MHz and sufficient qualitative fitting up to 1 GHz.

The known drawbacks of the method and possible model applications for alternative purposes are discussed.

Acknowledgment

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