Comparability of RF Immunity Test Methods for IC Design Purposes

Sergey Miropolsky, Stephan Frei
Technische Universität Dortmund,
Dortmund, Germany
sergey.miropolsky@tu-dortmund.de

***Abstract* — The differences between DPI and BCI tests in automotive IC-immunity testing are analysed. An approach, how to transfer results between the methods is shown on the example of a simple analogue IC. High conformity of the results for both tests (DPI and BCI) can be observed. The virtual RF immunity test is described, where the detailed modelling of the test setups is avoided and only the nearest IC environment (PCB and IC package) are modelled with high accuracy. The test can easily be implemented during the design process, and thus the reliability of the designed ICs can be significantly improved.**

Keywords: RF Immunity, Bulk Current Injection, BCI, Direct Power Injection, DPI, Virtual Tests

I. INTRODUCTION

Nowadays in automotive electronics the electromagnetic compatibility is a critical factor for general IC reliability. Several test methods have been standardized to verify the RF immunity on IC-level. Most common are the Direct Power Injection (DPI) [1] for ICs and Bulk Current Injection for ICs [2] and Systems [3]. With virtual tests the RF immunity of a designed IC can be predicted during the early design stage.

Still, the comparability of test methods remains unclear. Different criteria for maximum power levels are used; different physical mechanisms are involved in power transfer from the source to the DUT, etc. In the end, an IC might pass the IC-level DPI test but fails one of the system level tests (e.g. BCI).

The implementation approaches for virtual RF immunity tests were investigated by multiple research groups. Several models of the RF immunity test setups were introduced [4-9]. Still the simulation of the large-scale test setups like BCI doesn't help the general IC designer in the analysis of designed ICs, since any variation of the external test setup parameters results in another set of virtual test results.

In the current work the comparability of the two methods is discussed. An approach is proposed, where a good conformity of the results for DPI and BCI tests can be observed. A virtual RF immunity test is described, where the semiconductor model of the IC with a minimal amount of necessary external passive loads can be simulated up to 1 GHz. Thus the estimation of the test results can be performed.

II. RF IMMUNITY TESTS IN IC DESIGN

A. Direct Power Injection (DPI)

The DPI test [1] is simple and very effective. In the ideal case it may be considered that the RF power is directly coupled from a 50 Ohm RF source to the IC input pin through capacitive coupling and the IC response is observed.

The standard specifies the test setup to have a flat transfer function from the RF source to the IC with an allowed deviation less than 3 dB [1], when the IC is replaced with a 50 Ohm load. If there are resonances in the measurement, they can only be caused by the DUT input impedance. Thus the DPI results describe well the RF immunity of the DUT.

Several rather complex models have been developed for virtual DPI tests [4,5]. The models consider various PCB effects and power losses, the non-50 Ohm properties of the power injection system, etc. However, the application of these models in a virtual test may be complicated, since many setup parameters must be known.

B. Bulk Current Injection (BCI)

An alternative more complex RF immunity test is Bulk Current Injection. Here the RF power is injected as RF current into the cable system. This test method is widely used for testing larger systems with cable harnesses. The method is also used for RF immunity analysis of single ICs. The RF power is then injected into supply and ground cables at once. In this configuration the DUT is DC-grounded only through the cable harness, thus having only a weak capacitive connection to reference ground in HF range.

The RF power is injected as a common mode current into all cables in a bundle. The conversion between common and differential mode of the RF signal occurs due to the unsymmetrical termination impedances at the DUT side of cable. The differential mode RF signal is the resulting disturbance factor that affects the DUT. The transfer function of the test setup from the RF port to the DUT input pins is rather complex and shows many resonances due to large cable harness lengths. Also, due to high common mode levels, the DUT monitoring in the BCI measurement is possible only with optically decoupled probes.

Several simulation models have been developed for different BCI setups [6-9]. Due to the complexity of the models and large amount of setup-dependent parameters, the models are applicable only to some specific setup. It is usually not possible to predict even the transfer function accurately.

C. Comparability

The discussed methods use two different principles of the power injection. DPI uses direct capacitive coupling of the 50 Ohm system output to the IC pin at the PCB, thus having more or less flat transfer function in the higher frequency range. BCI instead uses current injection into a cable. This results in a much more complex transfer function with multiple resonances. Different physical limitations of forward power are usually used: constant forward power level in DPI vs. injection clamp calibration data in BCI.

However, in the end both methods provide some RF voltage amplitude at IC input pins. This is the resulting "disturbing factor" applied to the IC, and thus it can be used as a reference for the method comparison. The comparison of the methods is performed by analysing the dependence of the IC response on the RF voltage amplitude delivered to IC input at fixed frequencies. Thus comparing the transfer functions of the test setups can be avoided.

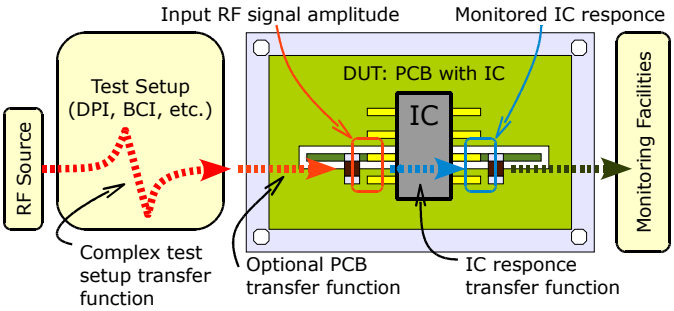

Figure 1. Transfer functions and effective input RF disturbance

III. DUT AND MEASUREMENT TECHNIQUES

A. IC Under Test

A simple analogue IC was used as a DUT. The chip function can be described as voltage regulator for a input battery voltage (6–24 V DC) into output digital supply voltage (3.3 V DC). The testchips were manufactured in a 0.35 µm CMOS technology.

The simple IC functionality allows defining an analogue quantity to characterise an IC failure. The DC level of output regulated voltage is observed and its shift under RF disturbance is measured. The dependencies of this output quantity on various input quantities, e.g. disturbance frequency or RF voltage amplitude at IC input pins, can be compared for different test methods, including virtual RF immunity tests.

By the shape of this failure curve the comparability of the methods can be analysed. It can be verified, if the IC shows similar reaction in both tests, e.g. either smooth output voltage deviation proportional to input disturbance or a complete malfunction at certain input level threshold and certain frequency.

B. Measurement in DPI Setup

The measurement of the DUT response was performed in the DPI setup. The IC was brought to the corresponding operating point. The constant forward power level was injected in the frequency range from 1 MHz to 1 GHz. The DC level at the output pin was measured at each frequency step. The RF signal amplitudes were measured at both input and output pins with active probes (LeCroy HFP2500, 0.7 pF || 100 kΩ, and LeCroy ZX1000, 0.9 pF || 1.0 MΩ) to be used later as a reference for method comparison.

For method comparison purposes the measurement was also performed at several fixed frequencies vs. injected power level. The dependencies of the output DC voltage on the input RF voltage amplitude were analysed.

C. Measurement in BCI Setup

DUT response was also measured in a BCI setup. To achieve better method comparability, no injection clamp calibration was performed. The constant forward power was injected into the clamp. The output DC voltage was directly measured with optically decoupled probe. Unfortunately, optically decoupled measurement methods for analogue signals are usually significantly limited in frequency range. Accurate and small optically decoupled probes for the GHz-range are not available. Thus the direct measurement of the RF signals was not possible.

To measure the RF levels a HF rectifier circuit based on a Shottky diode (fig. 2) was implemented. The monitored signal consisting of DC level (V_{DC}) and sinusoidal RF wave (V_{RF}) was rectified to another DC voltage (V_{MEAS}). This voltage could be measured with the optically decoupled probe. Under assumption that the initial RF wave is sinusoidal, the RF amplitude of the original signal can be extracted from DC level measurement.

To minimize the load on the measured node, no specific compensation parts for diode nonlinear effects were implemented. A measured correction factor was used for higher accuracy. The accuracy was verified at a PCB with 50 Ohm load, where the signal amplitude was exactly known. At the DC level of 10 V, the RF voltage amplitudes up to 8-10 V could be measured with 1 dB accuracy up to 1 GHz.

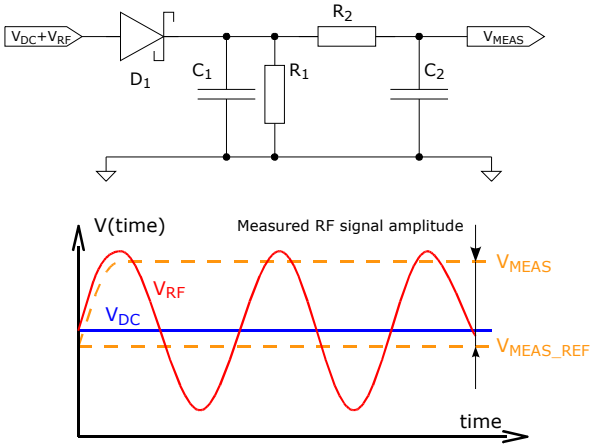

Figure 2. HF rectifier circuit as RF amplitude measurement method, D1 – rectifying diode, C1, R1 – circuit load and discharge current, R2, C2 – lowpass filter for the measured DC level

Using the proposed measurement method the RF voltage amplitude at IC input pin was measured in the BCI setup. Again, additional measurements were performed at several fixed frequencies vs. forward power. The dependence of the output DC voltage on the input RF amplitude was extracted.

IV. VIRTUAL RF IMMUNITY TEST

A. Overview

RF immunity simulations with complex IC circuits are important for IC design companies. Many accurate models for RF immunity setups have been developed. However, the virtual analysis of the IC RF immunity is limited by several requirements.

First, developing accurate semiconductor device models for RF application is complex and time consuming. This is not explicitly necessary to design the ICs which have basic functionality and operate in lower frequency ranges. Thus the accuracy of RF simulations may be unknown.

There are more specific requirements for the RF simulation models, which are normally not necessary for standard IC design. In the IC design the substrate of the chip and ground rails are usually considered to be always at zero potential. Thus they are normally modelled as a single node (common GND) in the circuit. For larger ICs this can lead to inaccuracy in higher frequency ranges, where more complex approaches are necessary. Moreover, the substrate node of integrated semiconductor devices can be implicitly assigned in a model to simulation reference ground, i.e. node 0 in SPICE-type software. This must be considered when these models are implemented within a larger RF setup, where the IC ground has some impedance to simulation reference ground.

The proposed simplification approach is to split the simulation of external large RF setup and the simulation of the IC itself. The splitting can be best performed at the IC package interface, since there the results can still be verified by measurements. The RF signals, either simulated in virtual test or measured in the physical test, can be applied directly to the simulation model of an IC with minimal necessary environment, and the simulated IC reaction can be obtained.

B. IC Netlist

The simulation model of the investigated voltage regulator IC was available as a circuit netlist. Functional models of the integrated semiconductor devices were available. The backannotation procedures were performed with the IC layout to extract the internal IC parasitics up to the bonding PADs of the die.

C. Passive IC Environment

Various methods have been considered as means to create the model of the passive IC environment. Often the 3D or so called 2.5D simulation is used for the PCBs, where the equivalent multiport S-parameter matrices are extracted from the PCB layout. These models can be later implemented in the test setup model as a subcircuit [10].

For the purposes of the experiment simplification, all the relevant signals were delivered to the IC at the designed PCB with equal 50-Ohm transmission line impedance traces. Thus, the small-signal measurement results could be easily deembedded up to IC pins. Afterwards, in the simulation model the 50-Ohm ports could be directly connected to the IC pins, and modelling of the PCB traces could be avoided.

Still the external impedances that could influence the RF response of the IC (e.g. the blocking capacitors) had to be modelled. Before the IC was soldered onto the PCB, the reflection measurements (S11) were performed for every such load, and the impedances were deembedded. The impedances were then approximated with passive equivalent RLC networks and implemented in the simulation model.

D. IC Package

It could be expected that the IC reaction in the immunity test is only dependent on the RF voltage amplitude at the input pins. However, several first simulation attempts have shown the second important factor. The input RF signal is coupled to the output pins through various paths. The RF signal level at output pin possibly disturbs the feedback circuitry and can also partly be responsible for the output voltage drops. To model these paths an accurate model for the IC package with bonding and external impedances was necessary.

Normally, 3D simulations are used for package modelling in the discussed frequency range [10]. This way of modelling is however significantly time consuming. To create a 3D model of the package the detailed data on package geometry and material properties are necessary.

In absence of this data, simple estimations of the bonding wire self-inductances still may be somehow performed. However, the accuracy of such estimations is not high enough to obtain acceptable correlation in the frequency range above 100 MHz, where most failures occur. Moreover, the inductive couplings between the pins, which play significant role in signal transfer, have to be considered.

In current work, to make sure that the virtual experiment results correspond to the real IC, the model of the IC package was based on measurements. The IC package was opened, and the die surface was covered with conducting paint (fig. 3). Thus all the semiconductor devices were short-circuited and the bonding wires were connected to each other at the IC level.

With several measurements the self-inductances and resistive losses were measured for every pin and bonding wire. The mutual inductances and inductive coupling coefficients were extracted by measuring the impedance of pins connected in parallel. The increase of the resistive losses in higher frequency range due to skin effect was considered with theoretical estimation and parameters were fitted to measurement results. Finally, by consequent removing the bonding wires from the package, the capacitive couplings between the package nodes were extracted.

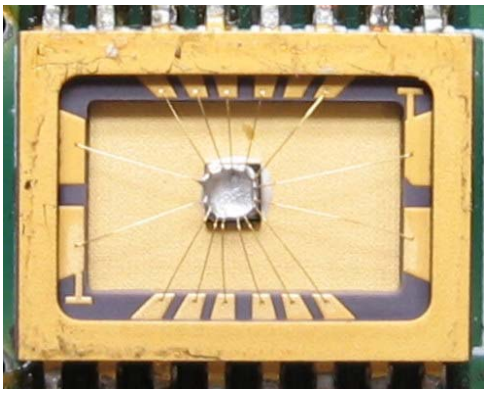

Figure 3. IC package opened for package properties measurements; the die surface is covered with conductive paint.

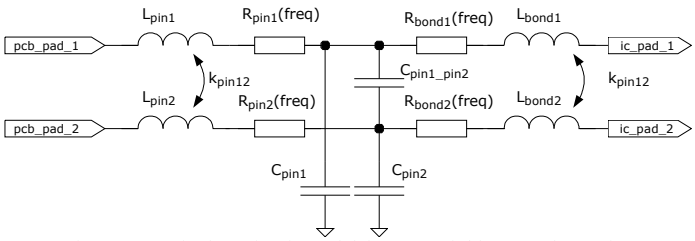

Figure 4. Equivalent circuit model for two neighbour package pins

The equivalent circuit for two neighbour pins is shown in fig. 4. The resistance model contains the frequency dependence according to a classic skin effect approximation. The entire package model is represented as a netlist and implemented in the final simulation model

E. Final model and small-signal verification

The final model is assembled as shown in fig. 5. The IC netlist is wrapped with package and PCB impedances. An RF signal source is attached to the input. The external RF amplitudes at the IC pins can be probed and compared to the measurements. The internal RF amplitudes can only be simulated and no comparison to the measurements is possible. The reference ground of the simulation is connected to the IC ground. The PCB ground is just another node in the simulation circuit, thus the external signals must always be sensed explicitly between the pin node and PCB ground.

Since the setup configuration in the virtual test is similar to DPI, the model can be verified by comparison to small-signal measurements. The input impedance of the IC is the dominating factor, which determines the input RF voltage amplitude during the test. Thus, it is the most important IC property that has to be verified with measurement. The signal transfer functions to output nodes may also be observed.

A multiple-port S-parameter measurement was performed; the dataset was deembedded up to the IC pins. The voltage amplitudes at IC pins were calculated from S-parameters and compared to simulation. The input impedance of the IC itself and together with the blocking capacitor was also extracted from S11 reflection and compared to simulation.

The results are shown in fig. 8, 9 and 10. Good fitting of the curves confirms the accuracy of the developed models.

F. Large-Signal analysis

The small-signal AC analysis can't be used to model the RF immunity tests, since the nonlinear properties of the semiconductor devices must be considered.

The common analysis type in the IC design is time domain transient analysis. However for a RF immunity test high frequency signals (above 100 MHz) must be simulated for quite large time periods (at least 1 ms is necessary for the IC to settle under RF excitation). This leads to drastic increase of simulation time, up to several hours for every frequency and forward power value.

The simulation was performed in Mentor Graphics ELDO RF [11]. A Steady-State (SST) analysis based on Harmonic Balance method was used to simulate the IC behaviour under RF excitation. The SST analysis computes the large signal steady-state of circuits stimulated by periodic signals. In other words, it directly computes the state reached by a circuit submitted to periodic large signal excitation when all transients have died out [11]. This is exactly what is required for the RF immunity simulation.

The frequency and power sweeps were performed within SST analysis, and both average DC levels and RF amplitudes at the nodes were extracted from the simulation results.

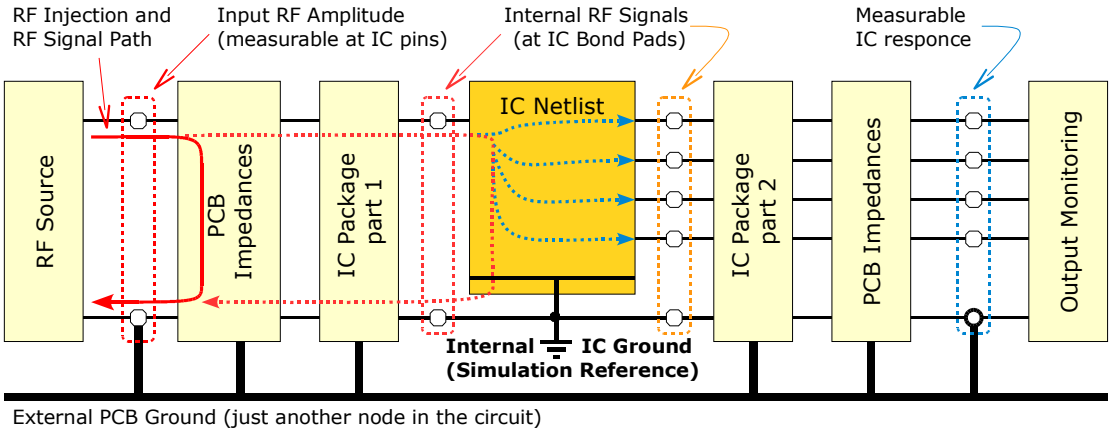

Figure 5. Block diagram of the RF immunity test simulation model

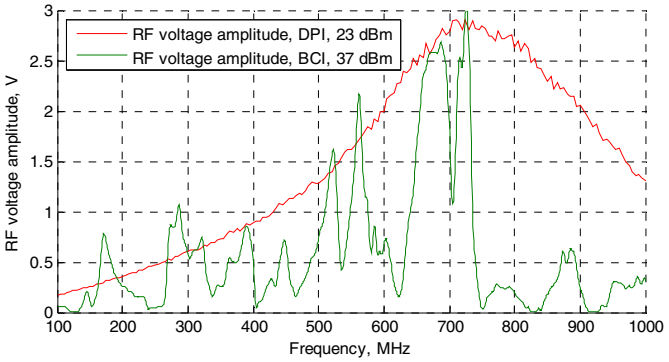

Figure 6. RF voltage amplitude delivered to IC input pin in DPI (23 dBm) and BCI (37 dBm)

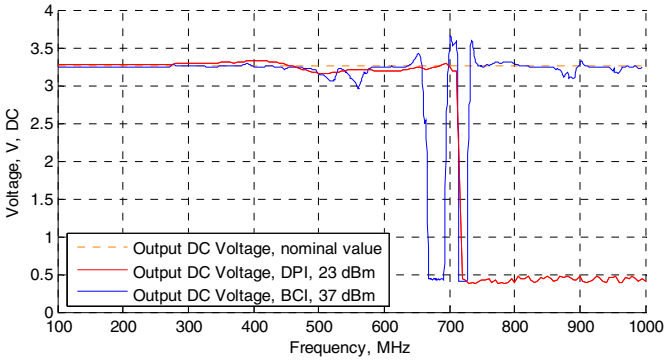

Figure 7. Corresponding IC response (output DC voltage) in DPI (23 dBm) and BCI (37 dBm)

V. Results And Discussion

A. *RF Immunity: Measurements*

The RF voltage amplitudes at the IC input pins measured in both DPI and BCI test are shown in fig. 6. The corresponding output DC voltages are shown in fig. 7.

The transfer function to the DUT input in DPI setup is rather smooth in the discussed frequency range of 100 MHz to 1 GHz. It is mostly determined by dominating impedance of the input blocking capacitor parasitic inductance (rising slope below 750 MHz) and capacitive IC input impedance (decay above 750 MHz). The profile of the RF level in BCI test is rather complex due to the multiple resonances in cable harness.

The overall power transfer from the RF source to the DUT in BCI setup is significantly low compared to DPI. At the highest resonance in BCI setup (around 700 MHz), injection of 37 dBm of forward power results in RF voltage amplitude at IC input pin of approx. 3.0 V. The same RF amplitude can be reached in DPI by applying only 23 dBm of forward power. This is however not a global rule, since it is dependent on multiple factors including the BCI setup configuration, harness lengths, resonance locations, etc.

By observing the IC response, i.e. the output DC voltage (nominal value about 3.3 V DC), the deviations under incident RF disturbance can be analysed. At lower disturbance levels the regulated voltage shows smaller deviations within tolerance range. When the immunity threshold is exceeded, a failure is observed, and the DC level falls to a level of about 0.4 V.

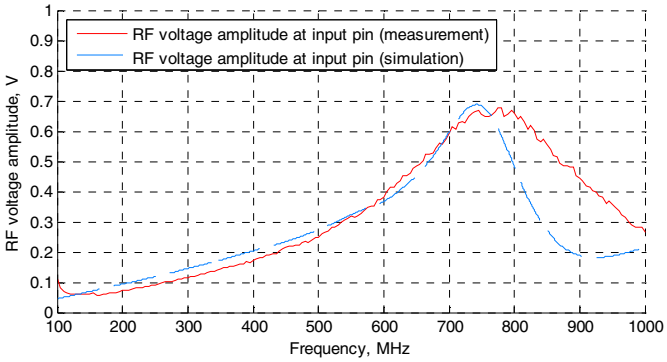

Figure 8. Input RF voltage amplitude small-signal measurement at 10 dBm vs simulation model

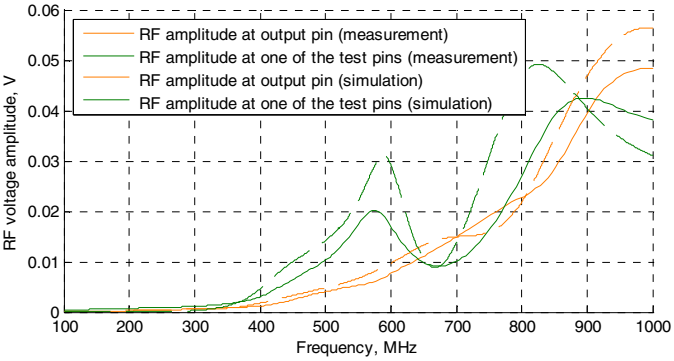

Figure 9. RF signal transfer to output pins, small-signal measurement at 10 dBm vs simulation model

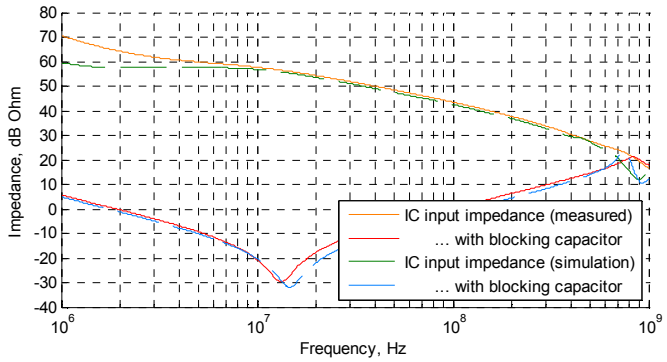

Figure 10. IC input impedance, measurement vs simulation model

Similar behaviour is observed in BCI test, except for the curve smoothness. The output follows the input RF level in the similar way as in DPI. Smaller deviations of same polarity are observed at different frequencies, where the RF level is below the failure threshold. The only significant failure is observed at resonance locations around 680 MHz and 725 MHz where the input RF level exceeds the tolerance limit due to a setup resonance.

To compare whether the dependence of output DC level to input RF levels is the same in both tests, the measured IC response was plotted against the RF voltage amplitude at IC pins for both tests for several frequencies. The curve shown in fig. 11 corresponds to one of the BCI resonance frequencies (725 MHz), where the highest RF voltage amplitude in BCI is observed.

The measured IC response has shown similar behaviour in both BCI and DPI tests (fig. 11). The injection mechanism (DPI or BCI) was only responsible for transferring the power to the DUT, either directly or through a complex setup with cable harness. This however assumes that the nearest IC environment doesn't change, i.e. same PCB or at least same PCB layout is used, no additional loads are attached to the DUT, same operating point of the DUT is used, etc.

B. Virtual RF Immunity Test Results

The IC response on the input RF disturbance for DPI, BCI and virtual RF immunity test at sample frequency of 725 MHz is shown in fig. 11. The output DC voltage is shown vs. input RF voltage amplitude at IC input pins.

The simulated IC response doesn't show those smaller deviations of the output DC voltage at lower RF levels (rise from 3.3 to 3.6 V at RF amplitude below 2.0 V). A possible reason is the IC ground behaviour, which cannot be modelled as an ideal reference node with zero potential anymore at the discussed frequencies.

At the same time the main IC failure with significant drop of output voltage was modelled correctly. As the simulation has shown, the RF amplitude threshold, where the failure has occurred, was significantly influenced by the coupling of the RF signal to the output node. The responsible model parameter was the dominating impedance of parasitic inductance of the pin and the blocking capacitor at the output node. This impedance was responsible for the rising RF amplitude at the output pin which probably disturbs the internal feedback circuitry. The further investigation of internal failure reasons is currently performed. However, with correct model parameters the output voltage failure can be simulated at the same input RF amplitude as in DPI and BCI. This is enough to obtain an overall RF immunity curve with sufficient accuracy.

The results are shown only for one sample IC in one sample configuration, and cannot be yet used for a global statement. However, the results prove that the virtual RF immunity tests can be successfully performed, even with normal semiconductor models, that weren't designed explicitly for high frequency range. The nearest passive IC environment (PCB and package) may bring much more distress to the results than the incompleteness of the semiconductor models in the high frequency range.

The results have also shown that for the accurate virtual testing of the ICs it is not necessary to develop accurate models of the large-scale RF test setups, like e.g. BCI. It is enough if the accurate model of the IC package and nearest external impedances and couplings is created. The RF level, equivalent to the one in a real test, may then be applied to the IC in virtual test and the awaited response can be obtained with sufficient accuracy.

VI. CONCLUSIONS

The comparability of two RF immunity test methods, DPI and BCI, has been analysed with a simple IC with analogue voltage regulator functionality. The RF voltage amplitude delivered to the IC input was observed as the intermediate input quantity. The shift of the regulated DC voltage from the nominal state is observed as output quantity. The failure behaviour of the device is analysed vs. the delivered RF voltage amplitude. In these terms a good conformity of the results for two different tests (DPI and BCI) can be observed. In the same terms the results can be transferred between the DPI and BCI for the ICs.

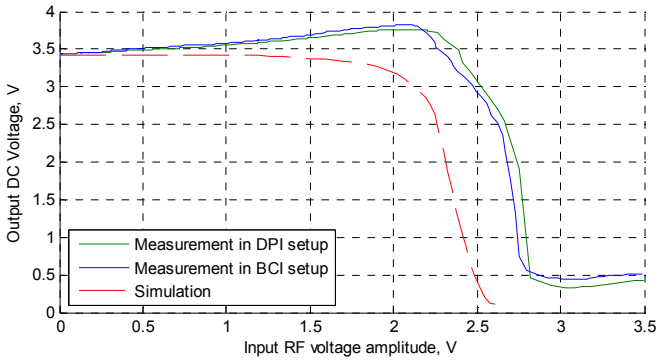

Figure 11. IC response at a sample frequency of 725 MHz (output DC voltage dependence on input RF amplitude) for DPI, BCI and virtual RF immunity test

A virtual RF immunity test approach is proposed, where the simulation model is simplified to the IC netlist with minimal amount of necessary external passive structures. Large-signal analysis based on harmonic balance is used to model the IC under external sinusoidal RF excitation. The virtual test results show good correlation with measurements in RF range. This virtual test can be fast and simply implemented during IC design phase. Thus possible failures can be found early, and costly IC redesign can be avoided.

REFERENCES

[1] IEC 62132-4: Integrated circuits - Measurement of electromagnetic immunity, part 4, Direct Power Injection.

[2] IEC 62132-3: Integrated circuits - Measurement of electromagnetic immunity, part 3, Bulk Current Injection.

[3] ISO 11452-4: Component test methods for electrical disturbances by narrowband radiated electromagnetic energy, part 4, BCI.

[4] A. Boyer, S. Bendhia, E. Sicard, "Modeling of a Direct Power Aggression on a 16bit Microcontroller Input Buffer", EMC Compo 2007, Turin, Italie (2007)

[5] R. Pedriau et al., "A Direct Power Injection Model for Immunity Prediction in Integrated Circuits", IEEE Tran. on EMC, vol. 50, no. 1, Feb. 2008

[6] M. F. Sultan, "Modeling of a Bulk Current Injection Setup for Susceptibility Threshold Measurements", IEEE Int. Symp. on EMC Proc., 1986, pp. 188-195.

[7] F. Grassi, F. Marliani, S. A. Pignari, "Circuit Modeling of Injection Probes for Bulk Current Injection," IEEE Tran., EMC 49, no. 3, Aug. 2007, pp. 563-576

[8] F. Lafon, Y. Belakhouy, and F. De Daran, "Injection probe modeling for bulk current injection test on multiconductor transmission lines," IEEE Symp. on Embedded EMC Proceedings, Rouen, France, 2007.

[9] S. Miropolsky, S. Frei, J. Frensch, Modeling of Bulk Current Injection (BCI) Setups for Virtual Automotive IC Tests, EMC Europe 2011, Wroclaw, Poland

[10] CST Microwave Studio - Reference Manual

[11] Mentor Graphics ELDO RF - Reference Manual