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Impact of Voltage Overshoots on ESD Protection Effectiveness for High Voltage Applications

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1

Biography

Yiqun Cao studied electrical and electronic engineering at the Rheinisch-Westflische Technische Hochschule (RWTH) Aachen in Germany. He received his Dipl. Ing. degree in 2007. The same year he joined smart power technology R&D at Infineon Technologies in Munich, where he is currently working on his Ph.D. thesis in close collaboration with the Institute for On-Board Systems Lab at the Technische Universität Dortmund. His field of research is ESD protection concepts in high voltage automotive technologies, with focus on chip- and system-level ESD.

2

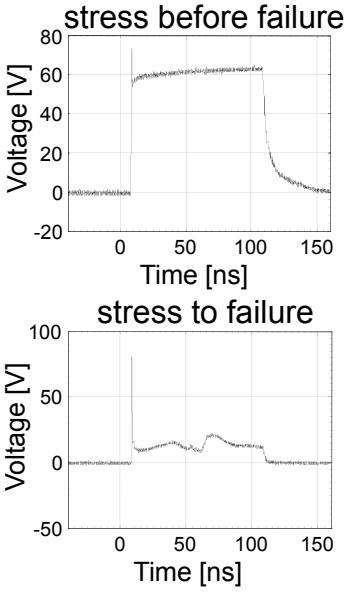
Abstract

Voltage overshoots due to turn-on behavior of ESD protection elements often show a negative impact on electro static discharge (ESD) hardness of the protected circuits. In the field of high voltage ESD protection, lateral DMOS (LDMOS) transistors are believed to be inherently weak due to the current localizations at the onset of triggering of the parasitic bipolar transistor [1-4]. LDMOS can be thus considered as being damaged when snapback occurs.

In this work, the n-type LDMOS (nLDMOS) transistors protected with pn-diode exhibit sensitivity to rise-time dependent voltage overshoots according to TLP results. The pn-diode, nLDMOS and the combination of the both circuit elements are investigated in detail. Even within very short time duration of the overvoltage caused by the finite reaction time of the avalanche breakdown diode, the parasitic bipolar transistor of the nLDMOS is still triggered, resulting in degradation of the total ESD protection effectiveness. Solutions for enhanced ESD protection using additional capacitance or secondary ESD protection concept are also presented. It is a must for designers to clarify the issues of harmful voltage overshoots since the studied circuit structures can be very applicable to the real ESD protection tasks.

3

Purpose



- pn-diode protected nLDMOS suffers from unexpected damage during TLP tests → why?
- Is the clamping of pn-diode too slow?
- Tests were performed without pre-pulse voltage. Do we have avalanche breakdown delay [5]?
- Are the ESD pulses with short rise-times critical for nLDMOS?
- How can we solve the overshoot problem by using ehanced ESD concepts?

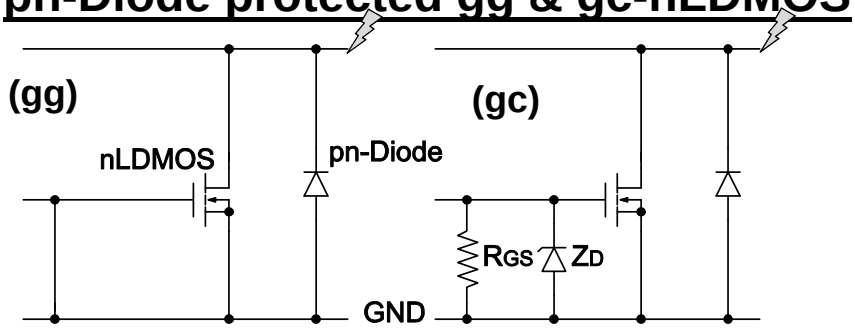
4

Outline

- Analyzed circuits
- Experimental results
- Study of dynamic issues of the circuit elements
- Influence in ESD protection effectiveness
- Solutions
- Conclusions

5

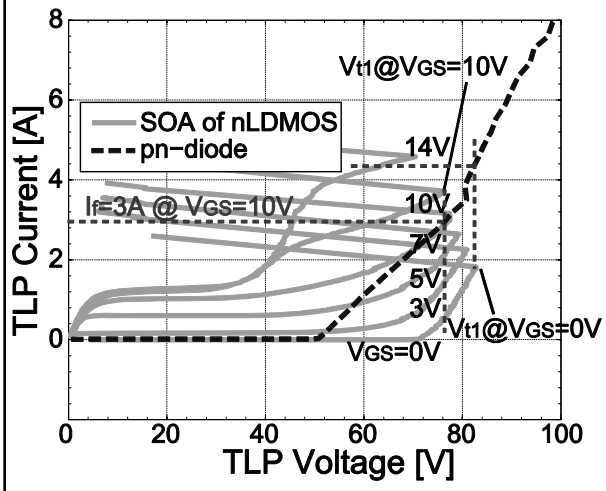
pn-Diode protected gg & gc-nLDMOS



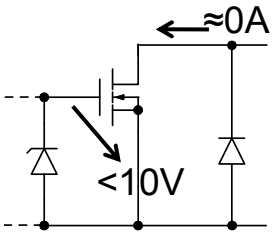
test structure	nLDMOS width	gate-biasing
small gg-nLDMOS	small	grounded-gate (gg)
small gc-nLDMOS	small	gate-coupled (gc)
large gg-nLDMOS	large (factor 68)	grounded-gate (gg)
large gc-nLDMOS	large	gate-coupled (gc)

6

Expectation of ESD Performance



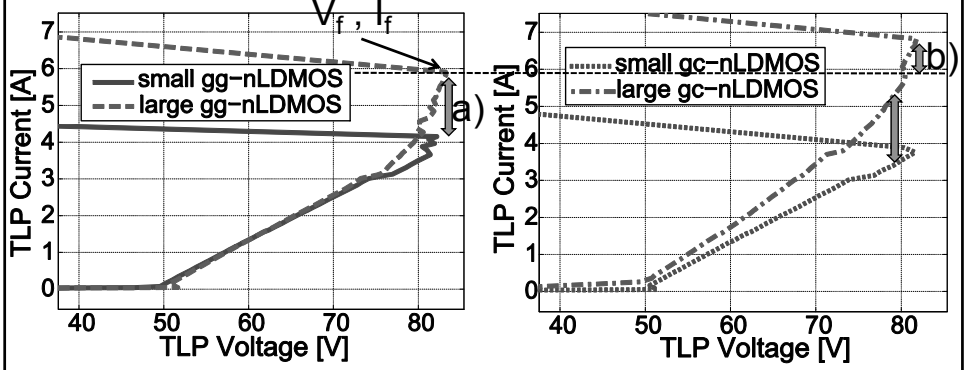
„worst case“: small gc-nLDMOS



At least 4kV HBM robustness (I_f=3A) expected

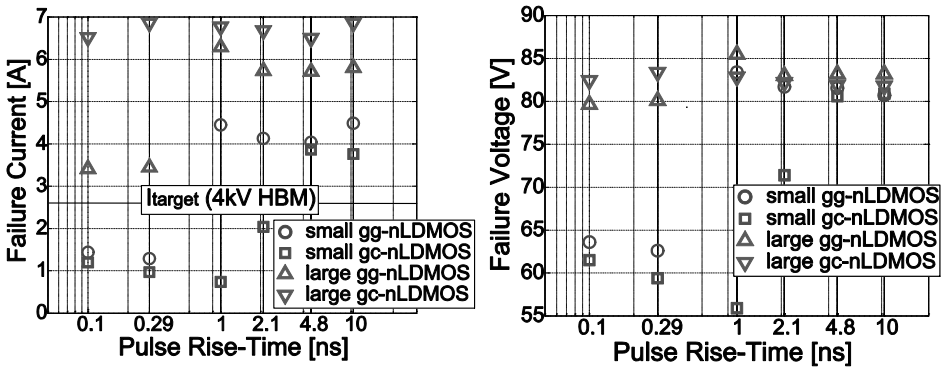
t_r = 10ns; t_w= 100ns; 70-90% averaging window

TLP Results with 10ns Rise-Time



- Different failure current:
  a) large vs. small b) gg vs gc
- All test structures showed expected ESD robustness → Is this really the case?

TLP Results with shorter Rise-Times

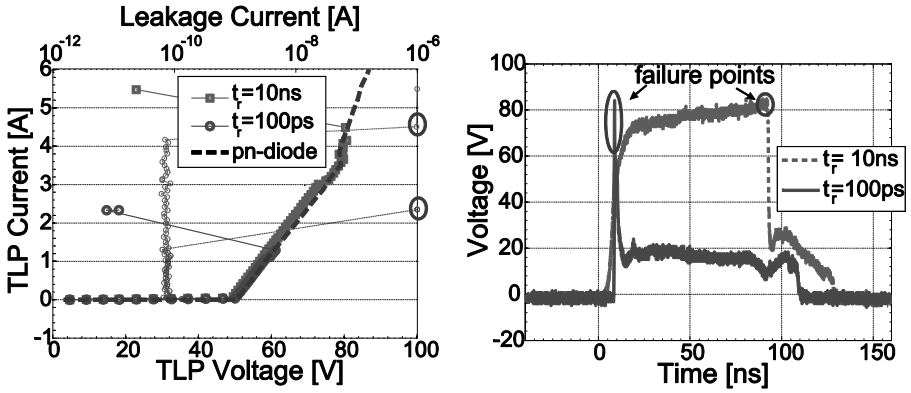


t_w= 100ns; 70-90% averaging window

- Except for large gc-nLDMOS, lower robustness was detected using TLP with shorter rise-times
- I_f, V_f of lower robustness fluctuated with repetitive testing

9

Two Failure Modes



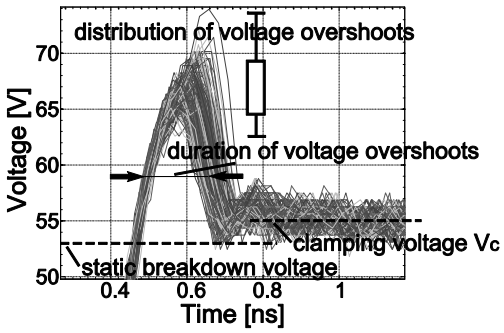
t_w= 100ns; 70-90% aver. window

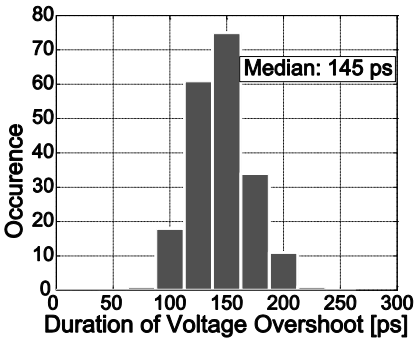
- Small gg-nLDMOS as an example
- Lower robustness identified with snapback at the beginning of the pulse → Why?

10

Voltage Overshoots of pn-Diode

- Initialization of avalanche multipication is random→ voltage overshoots
- 1A TLP current; 200 pulses → >10V overshoots



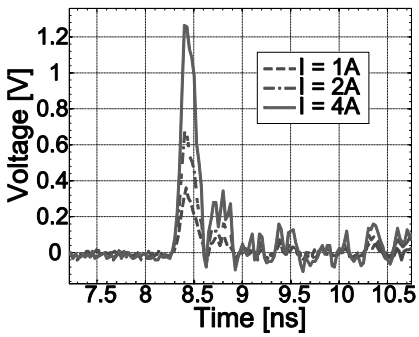


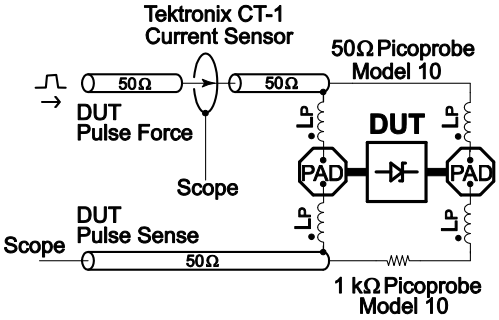
Were the overshoots test artifacts?

11

Test Artifacts

- 4-points probes method [6]
- Primary parasitics: inductive coupling



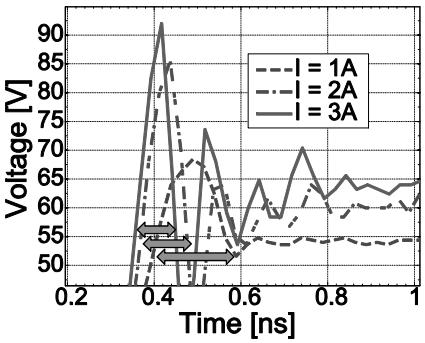


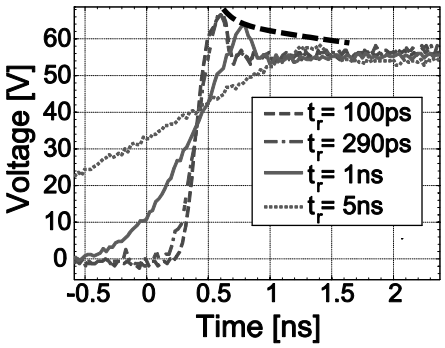
- Test artifacts verified with an on-chip short:
  - Good scalability
  - Small amplitude (~1V@4A)

Artifacts did not result in >10V voltage overshoots

12

Overshoot Dependency of pn-Diode





- t_r = 100ps, different I_{TLP}
- I_{TLP} ⬆ Amplitude ⬆ overshoot duration ⬇
- I_{TLP} = 1A, different t_r
- t_r ⬆ overshoot amplitude ⬇

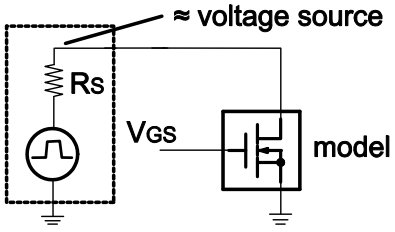
13

Voltage Conditioned Simulation

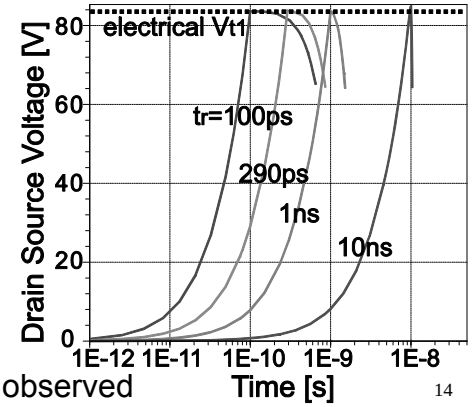
- 50Ω TLP source impedance

→Nearly a voltage source for small nLDMOS

→Voltage conditioned transient device simulation with small R_S



TLP simulation: V_{GS}=10V



No dependence of V_{t1} on t_r observed

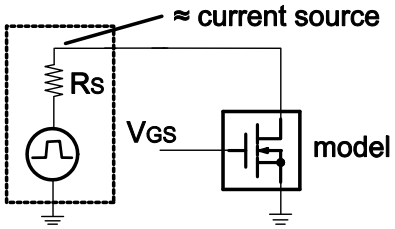
14

Current Conditioned Simulation

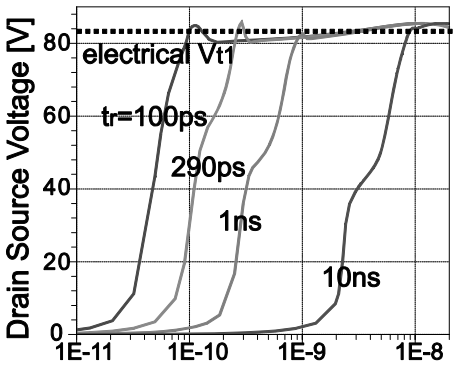
- 50Ω TLP source impedance

→Nearly a current source for large nLDMOS

→Current conditioned transient device simulation with large R_S

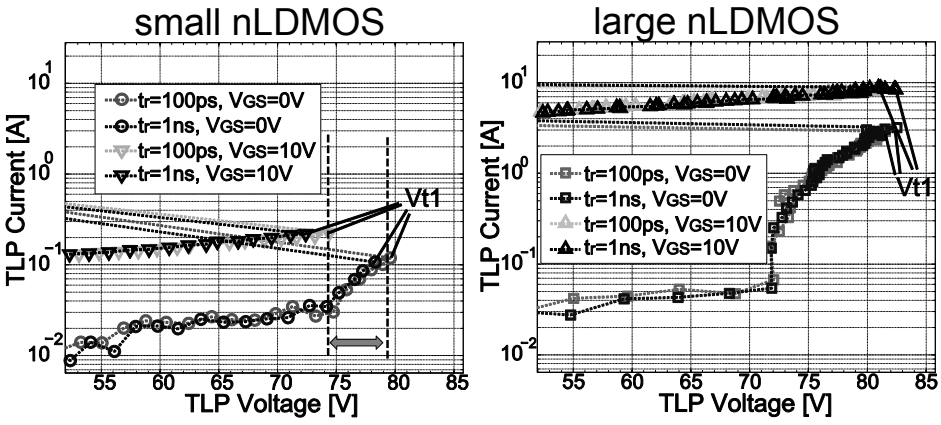


TLP simulation: V_{GS}=10V



No dependence of V_{t1} on t_r observed

SOA Data with short Pulse Duration

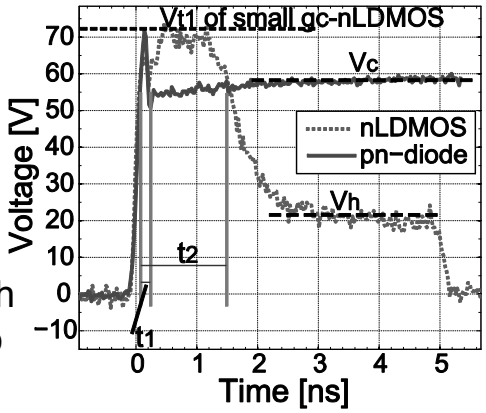


TLP data: t_w=5ns

- No significant difference of V_{t1} due to t_r observed
- Small gc-nLDMOS has the smallest V_{t1}

Is the pn-diode too slow?

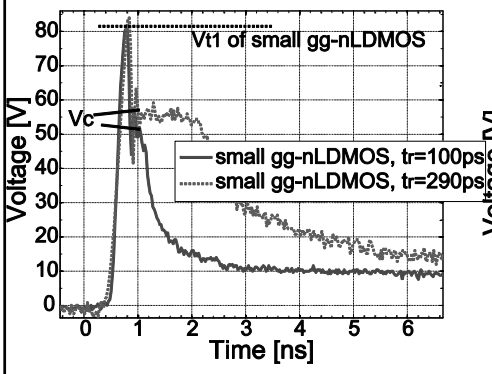
- Is the pn-diode too slow compared to the snapback process of the nLDMOS [7]?
- Very short TLP pulse (t_w=5ns) used to test snapback duration without damaging the nLDMOS
- t_1<t_2 → the pn-diode clamped voltage much faster but still failed to protect the nLDMOS

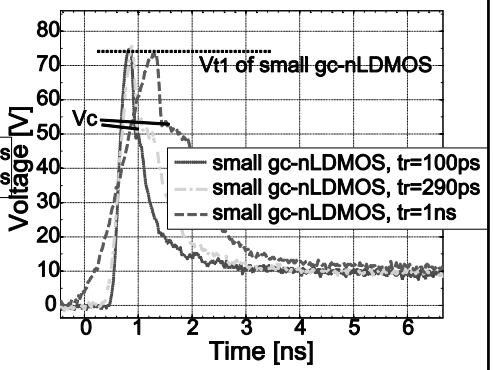


TLP data: t_r = 290ps

17

Influence of Voltage Overshoots



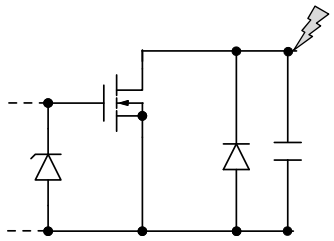


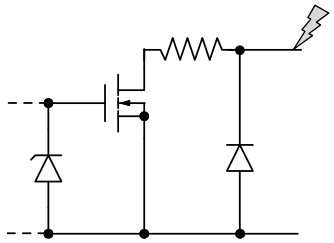
- Early failures at the pulse beginning
- Bipolar triggering in the nLDMOS cannot be turned off by the clamping of pn-diode on V_c

18

Improved ESD Solution with pn-Diode

- Add additional capacitance to enlarge t_r
  - 56pF improved weakest small gc-nLDMOS to withstand t_r=100ps TLP pulses to target level
- Enlarge the nLDMOS and add serial resistor to provide additional voltage headroom
  - Not always allowed in the real applications





19

Conclusions

- Avalanche pn-diode, nLDMOS and the combination are investigated in detail
- Two failure modes of analyzed circuits are identified
- ESD protected LDMOS transistors show sensitivity to extremly short voltage overshoots
- Improved ESD concepts using pn-diode and additional protection elements are given
- Further investigation of bipolar triggering issues in nLDMOS in dependence on V_{peak} and V_c is necessary

20

References

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[6] E. Grund, “VF-TLP wafer level performance based on probe needle configuration”, in Proceedings of 8th ESD Forum of the Interessengemeinschaft Electro Static Discharge e.V., Munich Germany, Dec. 2005, pp. 127-136.

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