Virtual ESD Testing of Automotive Electronic Systems

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***Abstract*— ESD events can cause numerous destruction effects in automotive electronic circuits. A prediction of ESD stress on system level is difficult and numerous iteration loops in the development process are necessary to fulfill the demands of automotive customers.**

A concept for system level ESD simulation is presented to predict robustness against ESD. Independent models of the different system components were developed and implemented, in order to build up a simulation process chain focused on ESD protection demands. The simulation method was characterized and compared with real measurements.

I. Introduction

Discrete electronic components and IC's are often not developed to withstand legal requirements and the demand of automotive customers. Substantial efforts were made on PCB level to minimize the risk of failure. Nevertheless, the risk is high for automotive ECU (electronic control units) to fail in ESD qualification tests. The root cause of inadequate ESD protection which leads to system failure is complex. The ESD robustness can often only be examined by expensive and time consuming tests on system level.

To avoid ESD failure on system level in many cases extensive protection strategies are applied. These protection strategies are limited to small sections of the system due to the complexity of ESD disturbance.

If the ESD design is finished once it can hardly be optimized on system level. Late optimizations cause higher costs, take effect on the functionality and enlarge the size of a device.

The whole pulse propagation chain beginning with the generation of high energy pulses until the destruction detection in an integrated circuit can be improved during development process by simulations of the current pulse propagation on system level.

II. Simulation Methodology

The simulation method must consider some basic requirements to ensure an effective simulation of ESD events. The models have to be exchangeable. They have to be executable on different computer systems and software architectures. VHDL-AMS seems to be an adequate simulation language to achieve these demands based on circuit simulation. The system should be divisible in independent sub modules to allow an adaptation to different requirements. Figure 1 illustrates a possible abstraction of a typical automotive test system for ESD qualification. The sub modules can be arranged free and enlarged depending on the specific requirements.

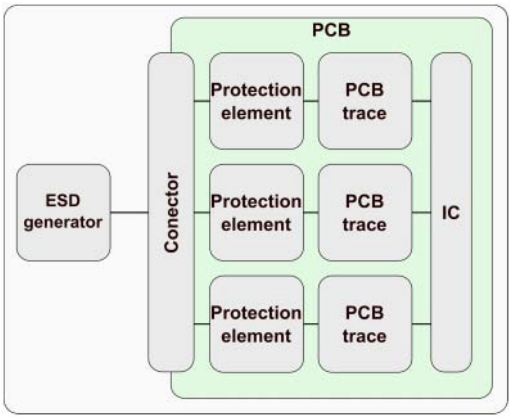

Fig. 1 Simplified block diagram of an automotive test system

III. Case Study

The simulation method is applied to a fictive electronic device, which represents a typical automotive ECU. The configuration is shown in Figure 2.

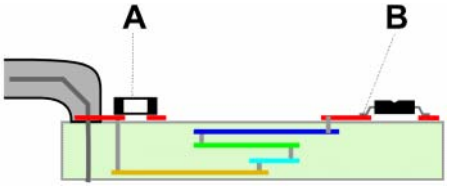

Fig. 2 Typical automotive ECU

For the development and verification of the method, only one ECU input pin was taken into account. The considered input connects an IC pin (B) with a wiring harness.

TABLE I
CARACTERISTIC OF A FICTIVE IC INPUT PIN

OFF impedance	2 kOhm
Input capacitance	< 1 pF
Max. DC voltage	65 V
Max. pulse voltage	250 V for 10 ns

For the ESD simulation relevant IC input pin data is shown in table I. The fictive IC input pin has to be protected with a discrete element (A) against a DC voltage level higher than 65 V and against pulse stress voltages higher than 250 V. The ECU input should withstand two ESD requirements as shown in table II. Two possible protection elements are selected in advance as shown in table III, a cheap capacitor and a more

expensive varistor. A cost optimized solution regarding the ESD requirement should be worked out.

TABLE II
ESD REQUIREMENTS

ESD generator discharge	IEC 61000-4-2 4 kV, contact mode 330 Ohm, 150 pF
Cable discharge event	1 m wire 5 cm over GND 2 kV charging voltage

TABLE III
POSSIBLE PROTECTION ELEMENTS

Capacitor	6,8 nF, 0603, X7R
Varistor	CT0603K14G

To select the best protection element without simulation a time consuming measuring process in a specialized laboratory is necessary. The selection of the protection element should be done, according this proposal, by simulation.

IV. SIMULATION SETUP

Figure 3 shows a basic arrangement of single simulation sub modules to adapt the simulation to the test setup.

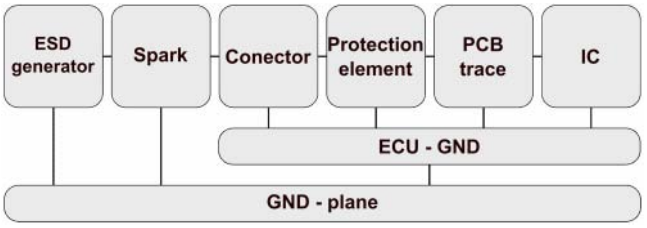

Fig. 3 Simulation setup for a virtual ESD testing

A. ESD Generator

IEC 61000-4-2 ESD generators are available from different manufacturers for testing and generation of ESD. These generators have different current pulse shapes, in spite of IEC standard conformity, and may lead to different results in ESD testing. A model for a Noiseken ESS-2000 ESD source was used in the simulation. The ESD source model consists of discrete RLC elements as described in [4]. For the CM (cable model) discharge [3] a lossy transmission line was used. Additional source models for Teseq, Noiseken and Schloeder ESD generator are available for simulation.

B. Spark

The time depending resistance and inductivity of the spark was modelled based on [3] and [5] with a linear closing switch and a discrete inductance for the spark.

C. Connector

The connector can not be neglected for the simulation due to its mechanical dimension. It can be modelled in many cases depending on the connector length as discrete inductivity as described in [6].

D. Protection element

1) Capacitor

The capacitor was modelled with an RLC circuit.

2) Varistor

The behaviour of the varistor can not be described with simple RLC elements. The non linear behaviour was characterized with leakage- and high current measurements. The measured data can be used as I/V curves in a model as described in [2].

E. PCB structure

The PCB attenuates an ESD pulse and can change the shape due to the low pass property and reflection behaviour of the PCB. The PCB can be modelled using analytical formulas or models from a field solver simulation, based on layout data [6].

F. ESD IC model

The IC input was simplified to an ideal resistor with 2 kOhm in parallel to a 1 pF capacitor. The input voltage at the IC pin was observed and used to benchmark the effectiveness of the ESD protection strategy.

V. MEASUREMENT SETUP

To verify the quality of the simulation results measurement were done using the same ECU testing configuration.

A. ESD test setup for IEC 61000-4-2

Figure 4 shows the used test setup, regarding to the IEC 61000-4-2 ESD standard [1]. For the discharge source (A) a Noiseken ESD generator (ESS-2000) was used. The ESD generator was attached to the test ECU via a connector (B). The selected protection element (C) was soldered near the connector.

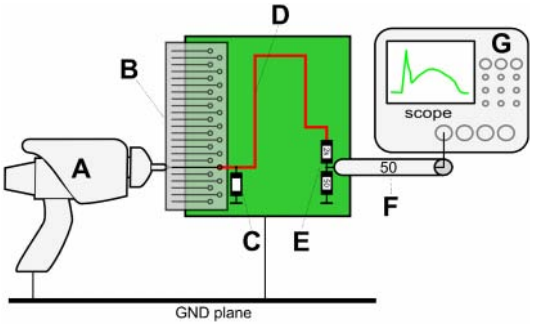

Fig. 4 Test setup for an IEC 61000-4-2 test

A six layer PCB trace (D) joins the connector with a virtual IC input structure. The voltage at the virtual IC input (E) was recorded by a 6 GHz oscilloscope (G) LeCroy SDA6000A. The oscilloscope was attached to the PCB by a Semi-Rigid cable (F). The IC input structure was substituted by a 2 kΩ resistor in series with a 50 Ω resistor.

B. ESD test setup for an cable discharge

Figure 5 shows the used test setup for CM verification, regarding to [3]. For the discharge source a charged wire (H) on

a 5 cm foamed polystyrene plate (A) was used. The wire was charged and then immediately attached to the ECU connector (B) with the appearance of a spark (I). The selected protection element (C) was soldered near the connector. A six layer PCB trace (D) joins the connector with a virtual IC input structure. The voltage on the IC input (E) was recorded by a 6 GHz oscilloscope (G) LeCroy SDA6000A. The oscilloscope was connected to the PCB by a Semi-Rigid cable (F). The IC input structure was substituted by a 2 kOhm resistor in series with a 50 Ohm resistor.

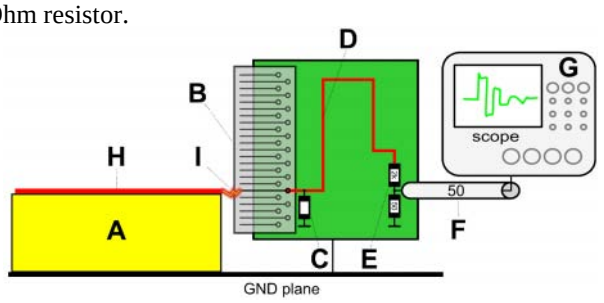

Fig. 5 Test setup for a cable discharge

VI. Comparison of Simulation and Measurment

A. ESD generator discharge

1) Varistor CT0603K14G

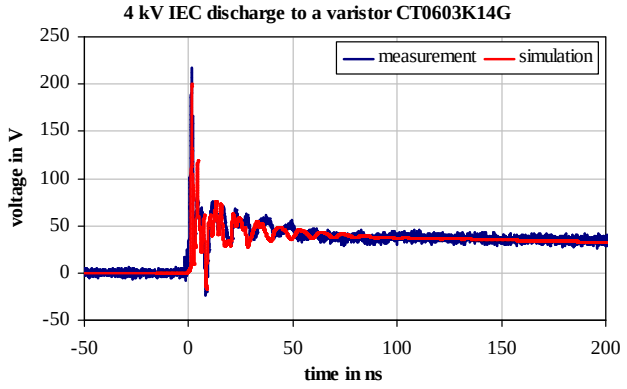

Fig. 6 Comparison of simulation and measurement of a 4 kV IEC discharge into an automotive ECU pin, protected by a varistor CT0603K14G

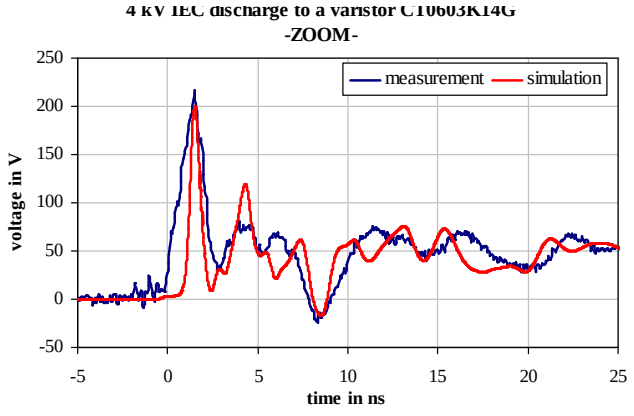

Fig. 7 Comparison of simulation and measurement of a 4 kV IEC discharge into an automotive ECU pin, protected by a varistor CT0603K14G

Figures 6 and 7 compare simulation and measurement data of an IEC 61000-4-2 discharge (4 kV, 150 pF, 330 Ohm) to the described device, protected by a varistor (CT0603K14G). The simulation shows a good correlation with the measurement data.

2) Capacitor 6,8 nF

Figures 8 and 9 compare simulation and measurement data of an IEC 61000-4-2 discharge (4 kV, 150 pF, 330 Ohm) to the device, protected by a 6,8 nF capacitor. An insignificant deviation is visible. This can be explained by a voltage depending capacitance behavior of the real protection device, which is not considered in the simulation model. The correlation of the peak voltage shows good results.

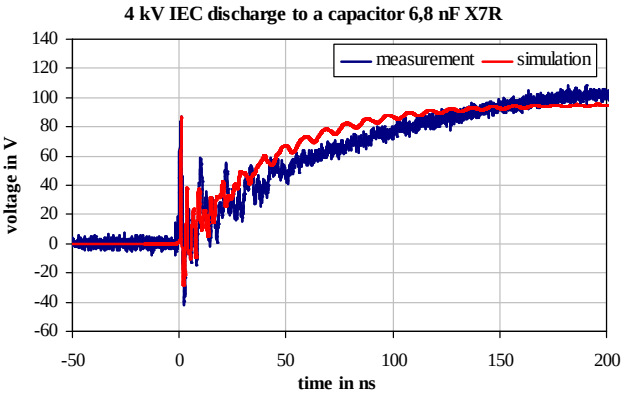

Fig. 8 Comparison of simulation and measurement of a 4 kV IEC discharge into an automotive ECU pin, protected by a capacitor 6,8 nF X7R

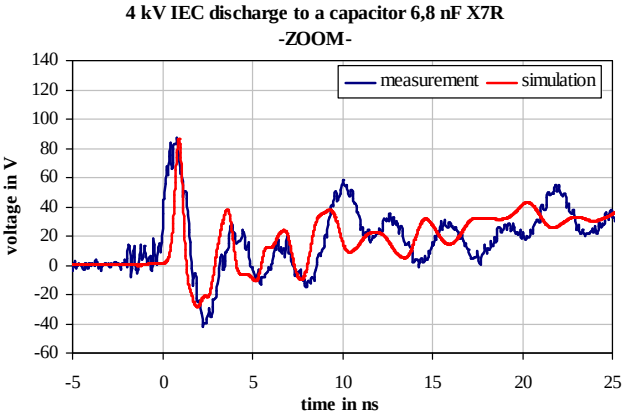

Fig. 9 Comparison of simulation and measurement of a 4 kV IEC discharge into an automotive ECU pin, protected by a capacitor 6,8 nF X7R

B. Cable discharge event

1) Varistor CT0603K14G

Figures 10 and 11 compare simulation and measurement data of a CM discharge (2 kV, 1m) to the device, protected by a varistor (CT0603K14G). Reflection effects are not considered correct for the spark due to the simplification of the spark to a linear closing switch and a discrete inductance. These explain a deviation in the peak voltage. Both pulses show a good agreement.

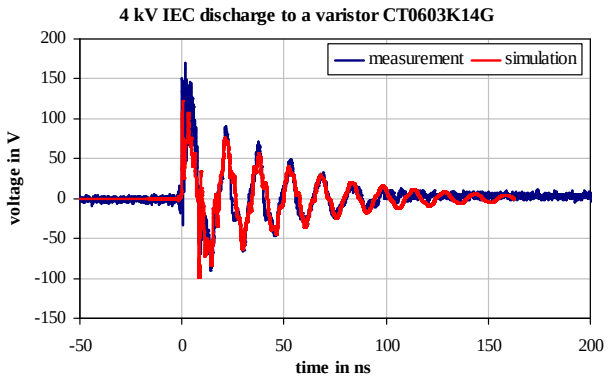

Fig. 10 Comparison of simulation and measurement of a 2 kV cable discharge event into an automotive ECU pin, protected by a varistor CT0603K14G

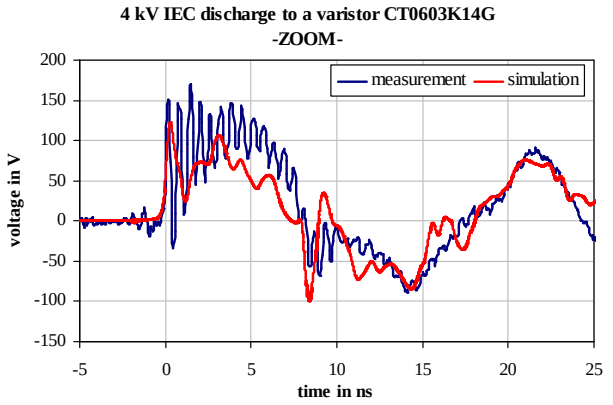

Fig. 11 Comparison of simulation and measurement of a 2 kV cable discharge event into an automotive ECU pin, protected by a varistor CT0603K14G

2) Capacitor 6,8 nF

Figures 12 and 13 compare simulation and measurement data of an CM (2 kV, 1m) to the device, protected by a 6,8 nF capacitor. A deviation in the peak voltage is visible similar to the varistor simulation before.

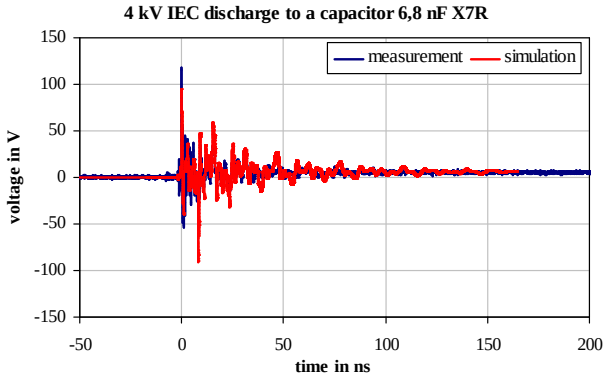

Fig. 12 Comparison of simulation and measurement of a 2 kV cable discharge event into an automotive ECU pin, protected with a capacitor 6,8 nF X7R

VII. USABILITY OF THE PROTECTION ELEMENTS

The investigated varistor is suitable to fulfill the requirements as regarded before. The 6,8 nF capacitor is not able to protect the IC pin from a maximum voltage level higher than 65 V if a IEC 61000-4-2 discharges is applied.

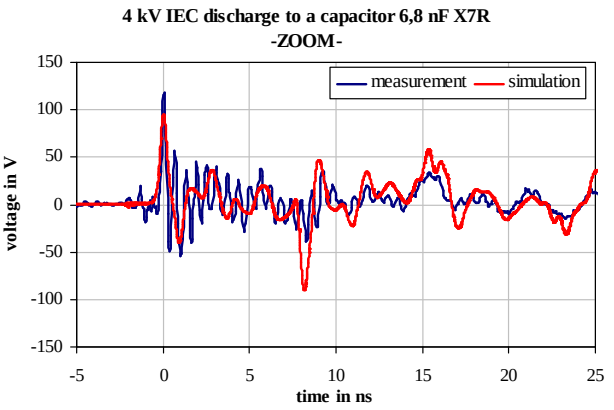

Fig. 13 Comparison of simulation and measurement of a 2 kV cable discharge event into an automotive ECU pin, protected with a capacitor 6,8 nF X7R

VIII. CONCLUSIONS

The introduced simulation method offers the possibility to validate and compare ESD protection concepts in advance. This allows a simulation of robustness and overvoltage impact due to ESD in an automotive electronic system.

The simulation results correlate well with measurement data. Protection concepts can be investigated without expensive and time consuming tests on system level. The decision of the suitability of a protection element can be done by simulation in advance. Furthermore the method leads to an improved understanding of complex PCB structures regarding ESD. An optimization without time consuming redesign of PCB structures is feasible. All this helps to reduce development efforts and to ensure product reliability.

Further work on an improved model for ESD behavior of IC input structures and an enhanced spark model is necessary.

IX. ACKNOWLEDGMENT

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